Myna II

Project code: 91.4C201.001
PCB REVISION: 05216-SB

CLK GEN.
IDT CV125
3

Mobile CPU
Dothan
CLE-1.5G / Dothan2.13G
(CPU on board,no socket) 4, 5

G792 19

HOST BUS 533MHz

DDR II
400/533 MHz 11,12

DDR II
400/533 MHz 11,12

400/533MHz

400/533MHz

Alviso-GM
KI.91501.017
6,7,8,9,10

LVDS
TV (EZ4 only)
LCD 13

RGB CRT
CRT 14

CH7307C 53 TMDS
DVI-D (EZ4 only) 35

DMI I/F 100MHz

ICH6-M
Ver. : B2, KI.80101.011
15,16,17,18

PCI BUS

TI
PCI 7411
1* Slot Cardbus
1* 1394
CardReader
24,25

PCMCIA I/F
PWR SW
TSP2220A 26
PCMCIA SLOT
Support TypeII 26

1394 6pin Conn 27

MS/MS Pro/ xD/ MMC/SD
5 in 1 26

Mini-PCI
802.11A/B/G
(only smaller) 30

LAN 22, 23
Giga
BCM5788-M

TXFM 23

RJ45 CONN 23

LPC BUS

NS SIO
87392 31

KBC
Renesas RE144B 30

BIOS ROM
4M BITS
PM49F004T-33VC 33

LPC
DEBUG
CONN. 33

FIR

Touch Pad 32

INT. KB 32

PATA

two USB port
on IO Board

USB
3 PORT 21

HDD 20

MINI USB
Blue-tooth 21

IO Board

(co-lay with PCMCIA)
New card 29
PCI-E

PWR SW
TPS2231 29

ACLINK

Codec
ALC655

Int. MIC
Mic In
Line In

Line Out
OP AMP
G1421B

INT.SPKR

MODEM
MDC Card

RJ11 CONN

IO Board

SYSTEM DC/DC TPS5130 41,42	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5 1D5V_S0 2D5V_S0(LDO)
SYSTEM DC/DC ISL6227 43	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3
TPS51100DGQ 43	
1D8V_S3	VTT_S0(0.9V)

MAXIM CHARGER MAX8725ETI 44	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 16.8V 3.2A UP+5V 5V 100mA

CPU DC/DC ISL6218CV-T 40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

Easy Port 4 (124 PIN)

AC IN | RJ45-11 | SEARIAL PORT | CRT | PRINTER | PS2 | MIC | LINE IN | LINE OUT | TV OUT | DVI | PCIeX2 | SMBUS

34, 35

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

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Custom	Myna II	SB

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Alviso Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott **1 = Dothan** (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled** (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V** (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

1.CHECK P5[1D5V & 1D5V-AVDD]
2.CHECK P8[PM & GM]

PCI Routing

	IDSEL	IRQ	REQ/GNT
7411	25	B.F.G	0
MiniPCI	21	E	1
LAN	23	E	2

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

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?cost

PCLK_PCM & PCLK_SIO
need equal length

CLK_ICH14 & CLK14_SIO
need equal length

SB_0817

H/L: 100/96MHz

H/L : CPU_ITP/SRC7

Dummy when no EZ4

Dummy when no new Card

EMI capacitor

IN (3D3V_S0)	EN (1907_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z

CFG2	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

IDTCV125PA

71.00125.00W

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator - IDT125

Size: A3 | Document Number: Myna2 | Rev: SB

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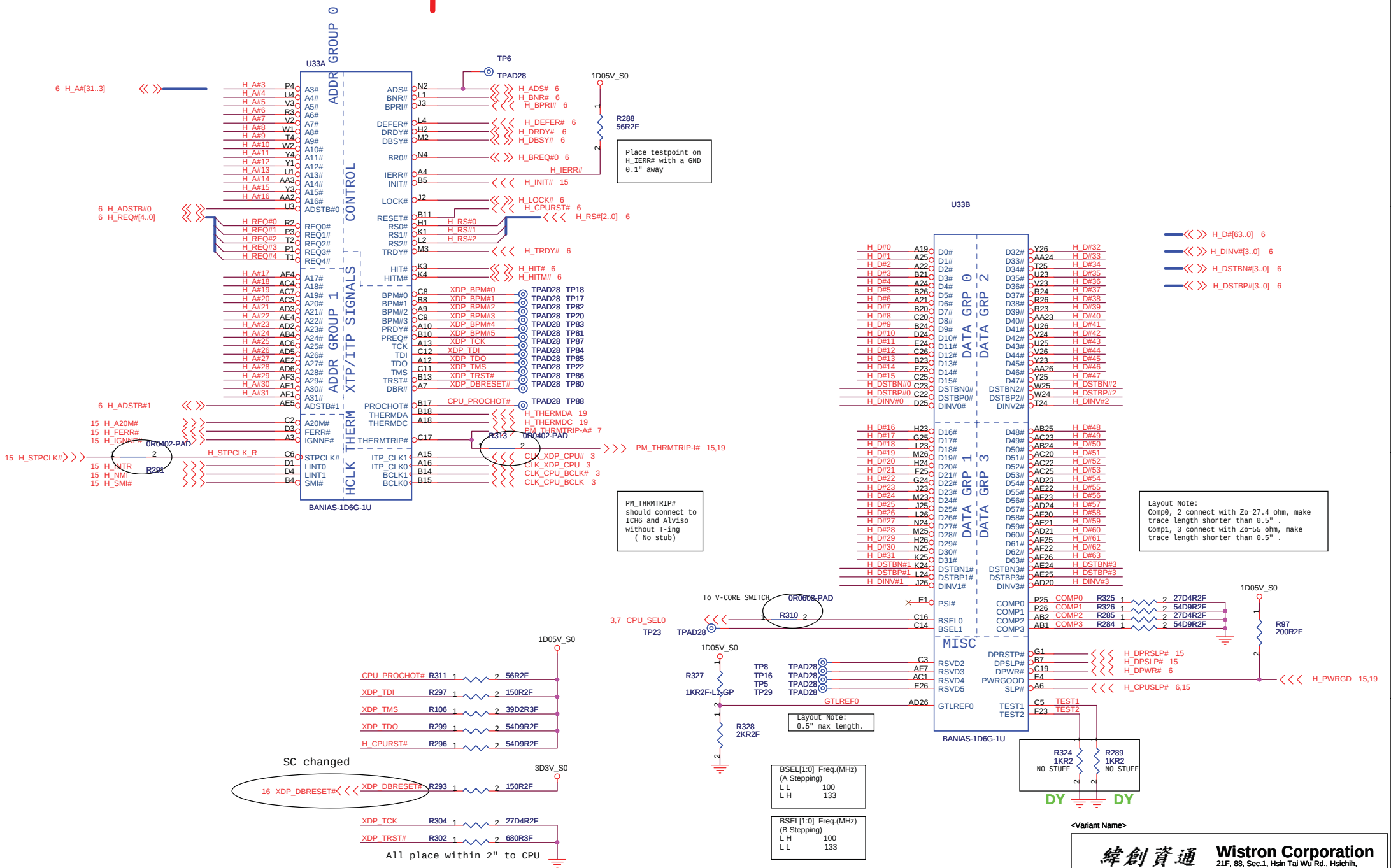

<variant_name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU (1 of 2)***	
Size A3	Document Number **Myna2**	Rev **SB**
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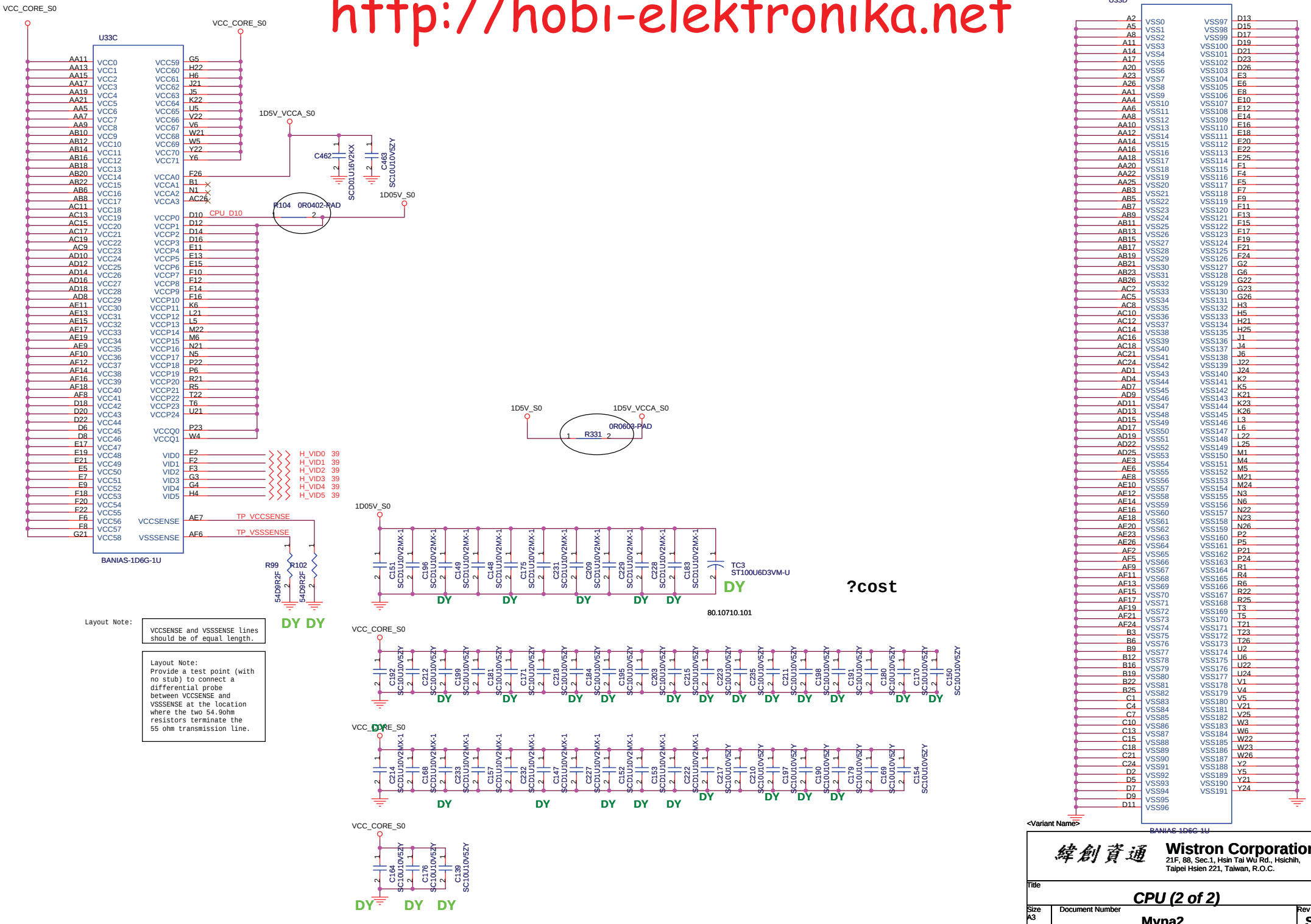

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (2 of 2)
Size A3	Document Number: Myna2
Rev	SB
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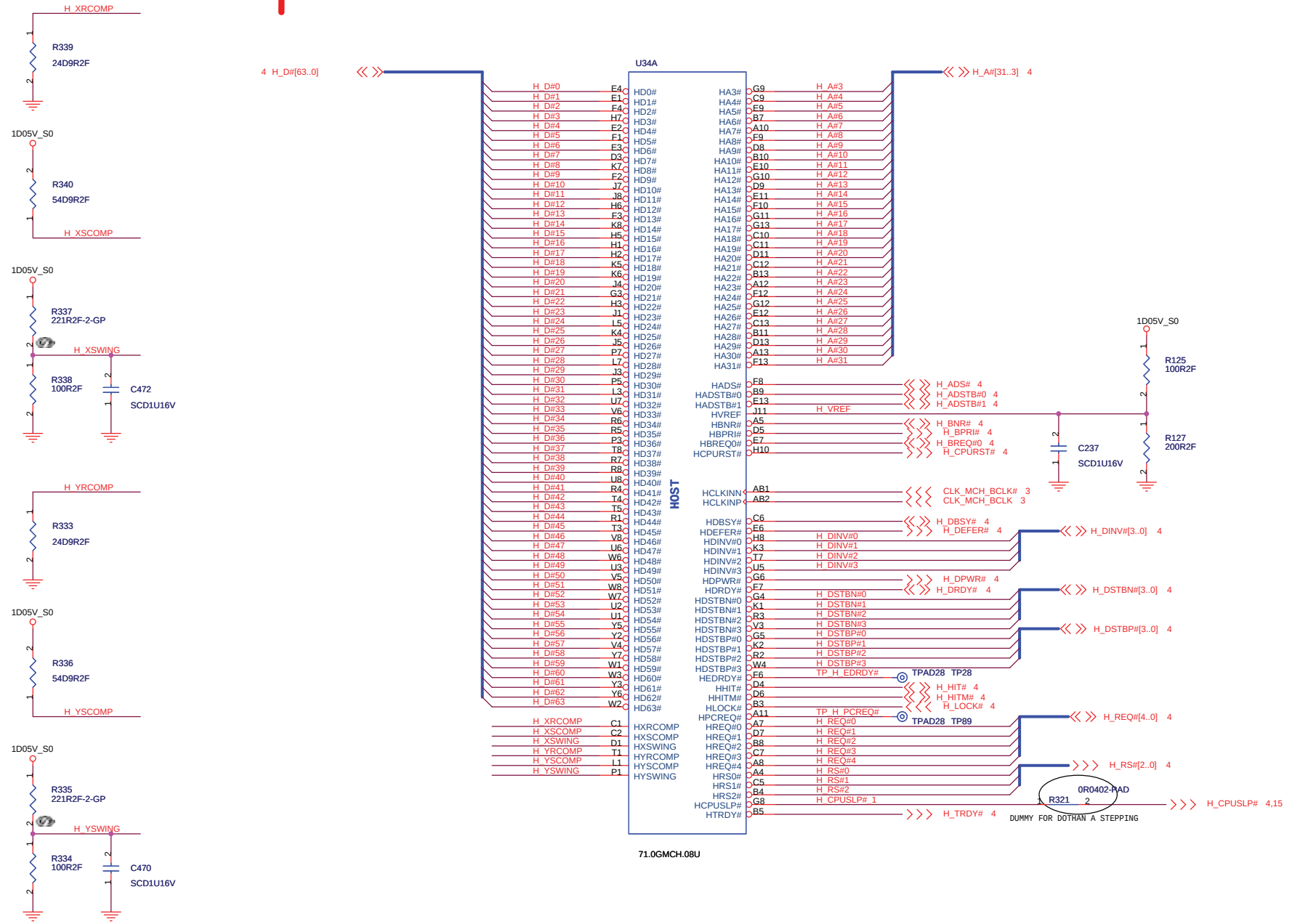

Place them near to the chip

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (1 of 5)

Size: A3 | Document Number: Myna2 | Rev: SB

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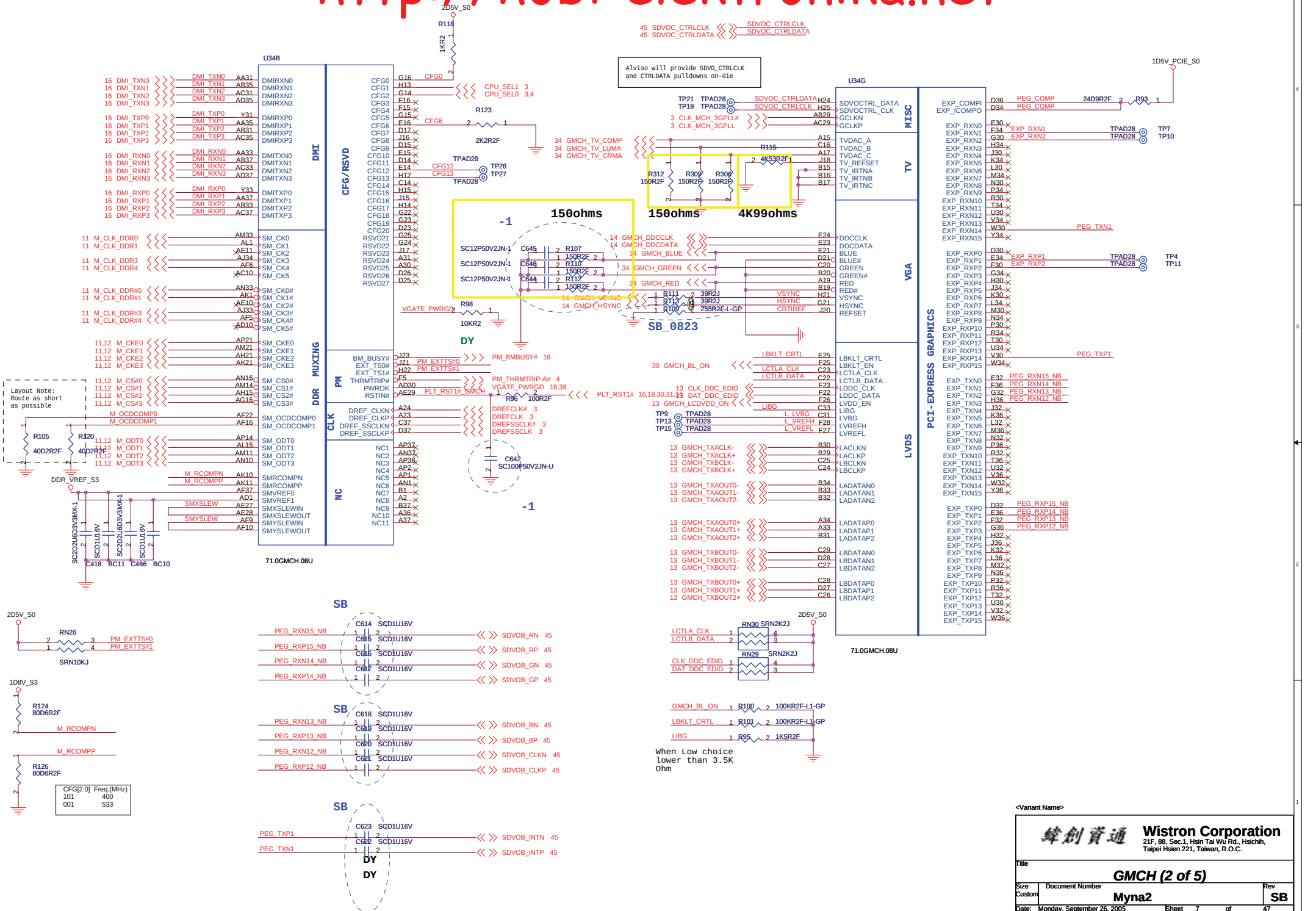

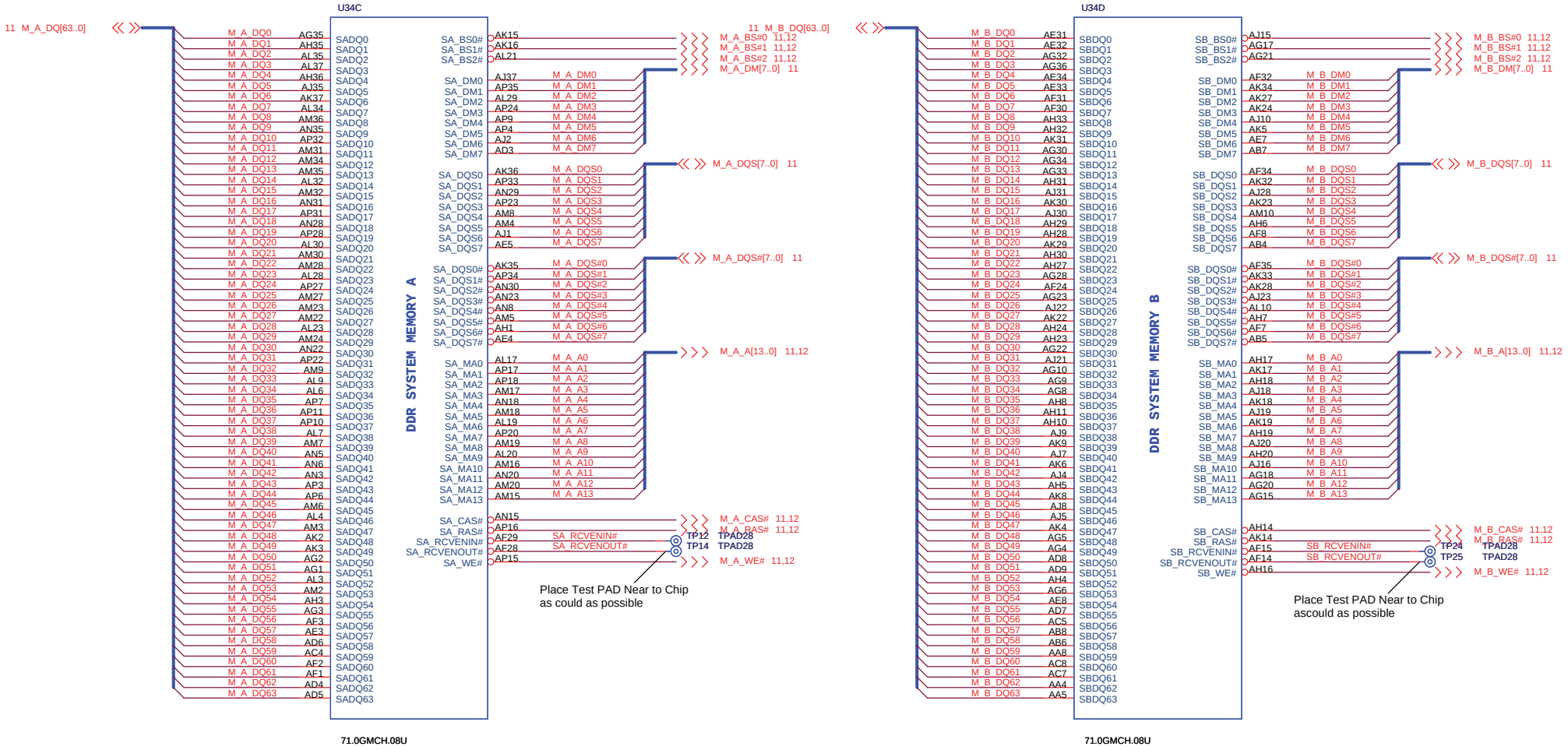

<Variant Name>

緯創資通 Wistron Corporation
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Title: GMCH (3 of 5)

Size	Document Number	Rev
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D1U10V2MX

D1U10V2MX
When PM replace to GM

Route ASSATVBG gnd from GMCH to decoupling cap groung lead and then connect to the gnd plane

VCC 1D05_S0 for low speed graphic clock.1D5V_S0 for high speed clock.default use 1D05V_S0

Note: All VCCSM pins shorted internally

Note: All VCCSM pins shorted internally

Route ASSA3GBG gnd from GMCH to decoupling cap groung lead and then connect to the gnd plane

U34E

71.0GMCH.08U

?cost

Graphic Freq. /Memory Freq.	1D05V	1D5V
200MHZ/DDR333	YES	YES
200MHZ/DDR2 -400/533	YES	YES
320MHZ/DDR2 -400/533	NO	YES

Layout Notes: VSSA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.

Route VSSA_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.

<Variant Name>

Wistron Corporation
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Title: GMCH (4 of 5)

Size: A3 | Document Number: Myna2 | Rev: SB

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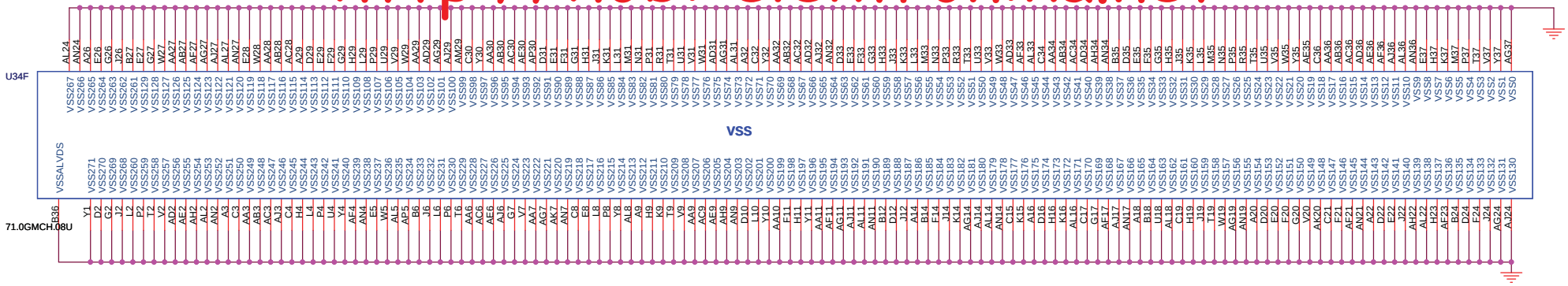
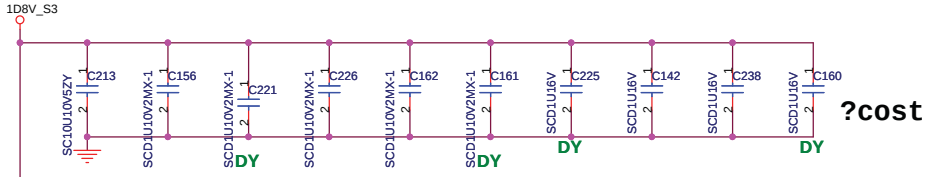
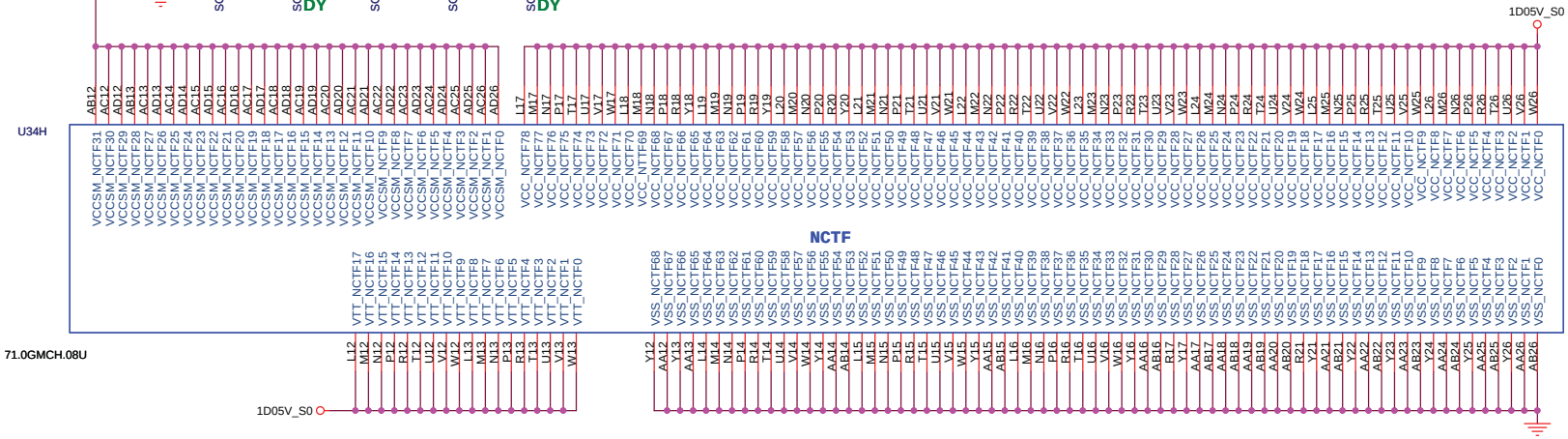


Place these Hi-Freq decoupling caps near GMCH





<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (5 of 5)

Size: A3 | Document Number: Myna2 | Rev: SB

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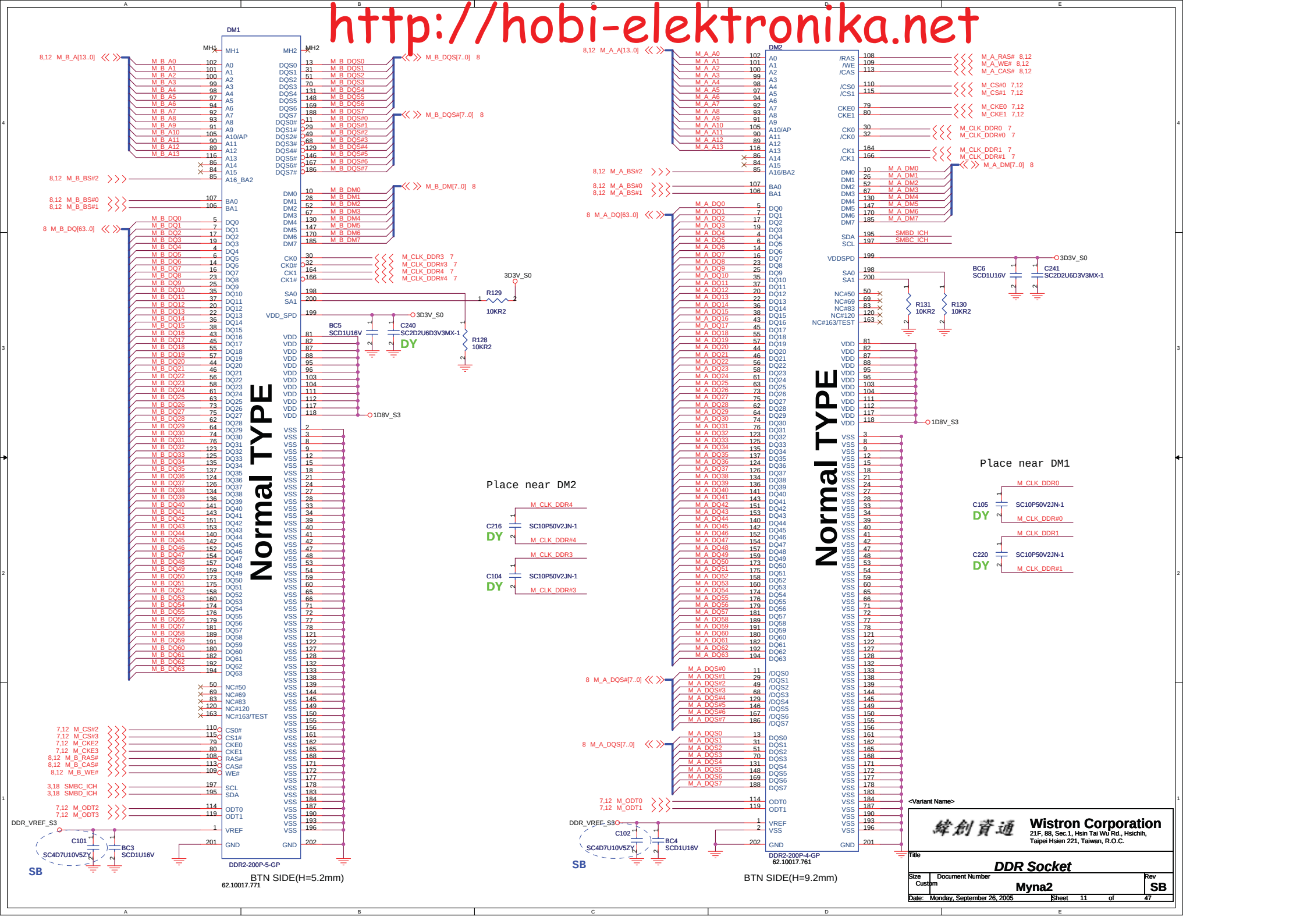

PARALLEL TERMINATION

VTT_S0

Put decap near power(0.9V) and pull-up resistor

RN53 — SRN56-1
M_CS#2 7,11
M_ODT2 7,11
M_B_A13
M_B_BS#0 8,11

M_A_A[13..0] 8,11
M_B_A[13..0] 8,11

R275 56R2F — M_CKE2 7,11
R274 56R2F — M_B_BS#2 8,11
R108 56R2F — M_ODT1 7,11
R94 56R2F — M_CKE0 7,11

RN49 — SRN56-1
M_B_A12
M_B_A8
M_B_A9
M_CKE3 7,11

RN52 — SRN56-1
M_B_A2
M_B_A0
M_B_BS#1 8,11
M_B_RAS# 8,11

RN51 — SRN56-1
M_B_A6
M_B_A4
M_B_A1
M_B_A10

RN50 — SRN56-1
M_B_A5
M_B_A3
M_B_A11
M_B_A7

RN54 — SRN56-1
M_B_WE# 8,11
M_B_CAS# 8,11
M_ODT3 7,11
M_CS#3 7,11

RN31 — SRN56-1
M_A_WE# 8,11
M_CS#1 7,11
M_ODT0 7,11
M_A_A13

RN27 — SRN56-1
M_A_A3
M_A_A0
M_A_A10
M_A_BS#1 8,11

RN23 — SRN56-1
M_CKE1 7,11
M_A_BS#2 8,11
M_A_A8
M_A_A9

RN28 — SRN56-1
M_A_BS#0 8,11
M_A_RAS# 8,11
M_CS#0 7,11
M_A_CAS# 8,11

RN24 — SRN56-1
M_A_A12
M_A_A6
M_A_A11
M_A_A7

RN25 — SRN56-1
M_A_A4
M_A_A5
M_A_A2
M_A_A1

Decoupling Capacitor

VTT_S0

Put decap near power(0.9V) and pull-up resistor

DY
C429 SCD1U16V
C427 SCD1U16V
C441 SCD1U16V
C430 SCD1U16V
C432 SCD1U16V
C434 SCD1U16V
C423 SCD1U16V
C421 SCD1U16V
C422 SCD1U16V
C438 SCD1U16V
C166 SCD1U16V
C173 SCD1U16V
C122 SCD1U16V
C125 SCD1U16V
C130 SCD1U16V
C127 SCD1U16V
C135 SCD1U16V
C133 SCD1U16V
C141 SCD1U16V
C131 SCD1U16V
C145 SCD1U16V
C158 SCD1U16V

1D8V_S3

Place these Caps near DM1

C132 SC2D2U6D3V3MX-1
C129 SC2D2U6D3V3MX-1
C140 SC2D2U6D3V3MX-1
C126 SC2D2U6D3V3MX-1
C123 SCD1U16V
C143 SCD1U16V
C120 SCD1U16V

1D8V_S3

Place these Caps near DM2

C439 SC2D2U6D3V3MX-1
C435 SC2D2U6D3V3MX-1
C431 SC2D2U6D3V3MX-1
C425 SC2D2U6D3V3MX-1
C424 SC2D2U6D3V3MX-1
C144 SCD1U16V
C124 SCD1U16V
C121 SCD1U16V
C117 SCD1U16V

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *DDR2 Termination Resistor*

Size: A3 | Document Number: Myna2 | Rev: SB

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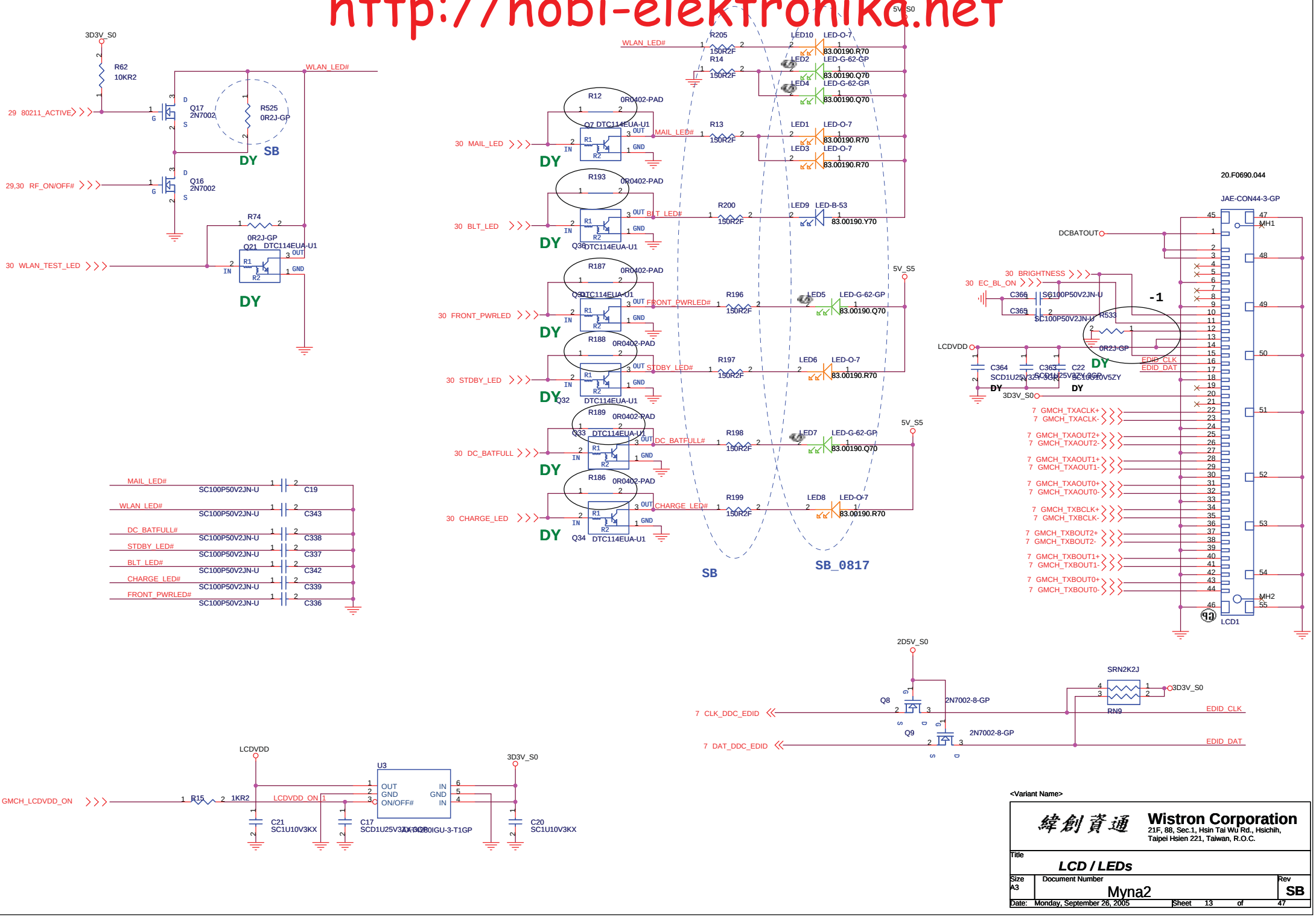

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***LCD / LEDs***
Size A3	Document Number: Myna2
Rev	SB
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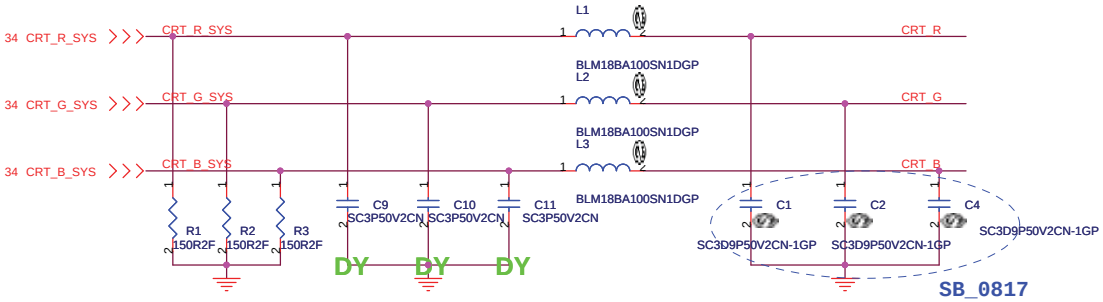

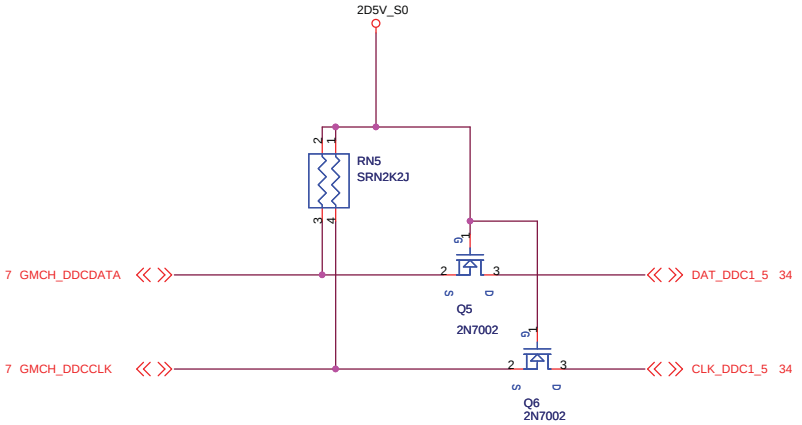

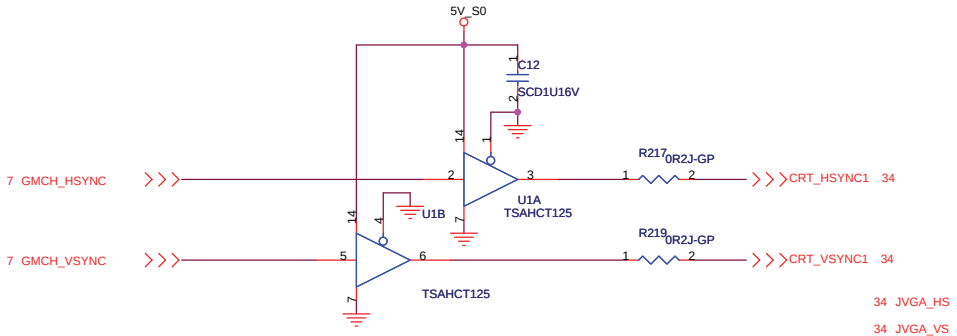

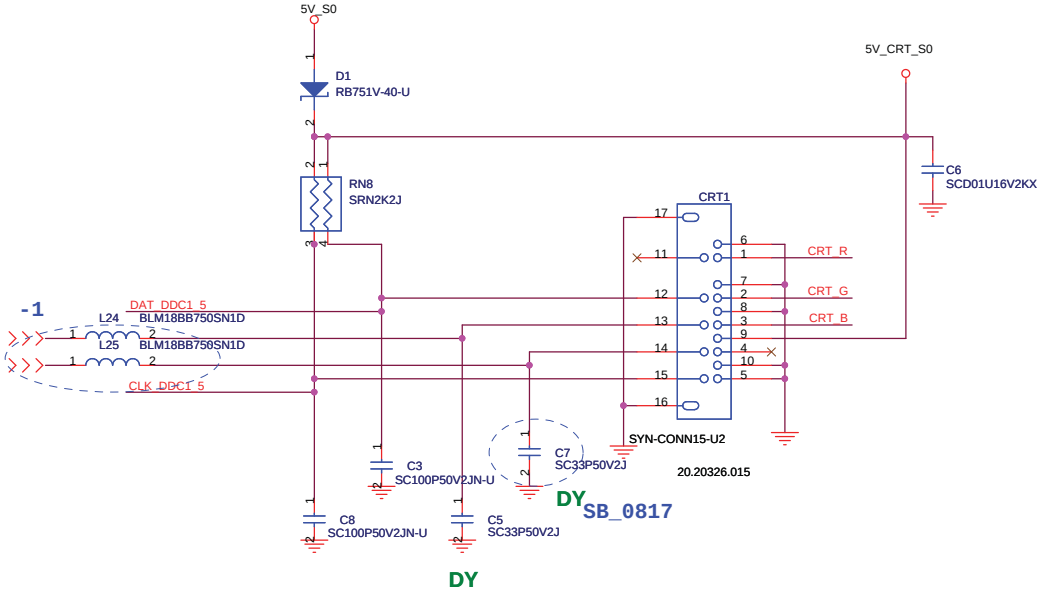

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CRT Connector		
Size: A3	Document Number: Myna2	Rev: SB
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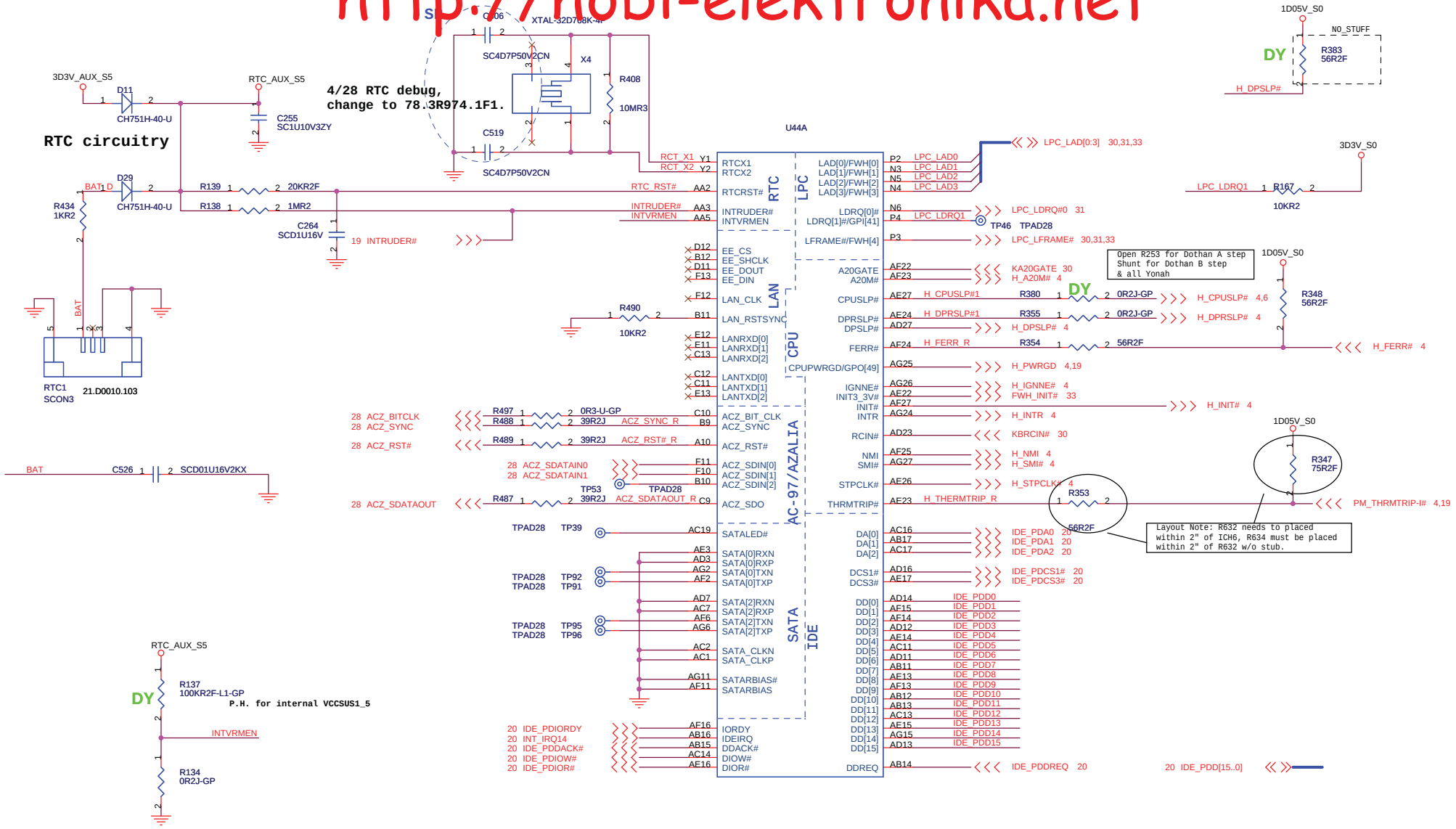
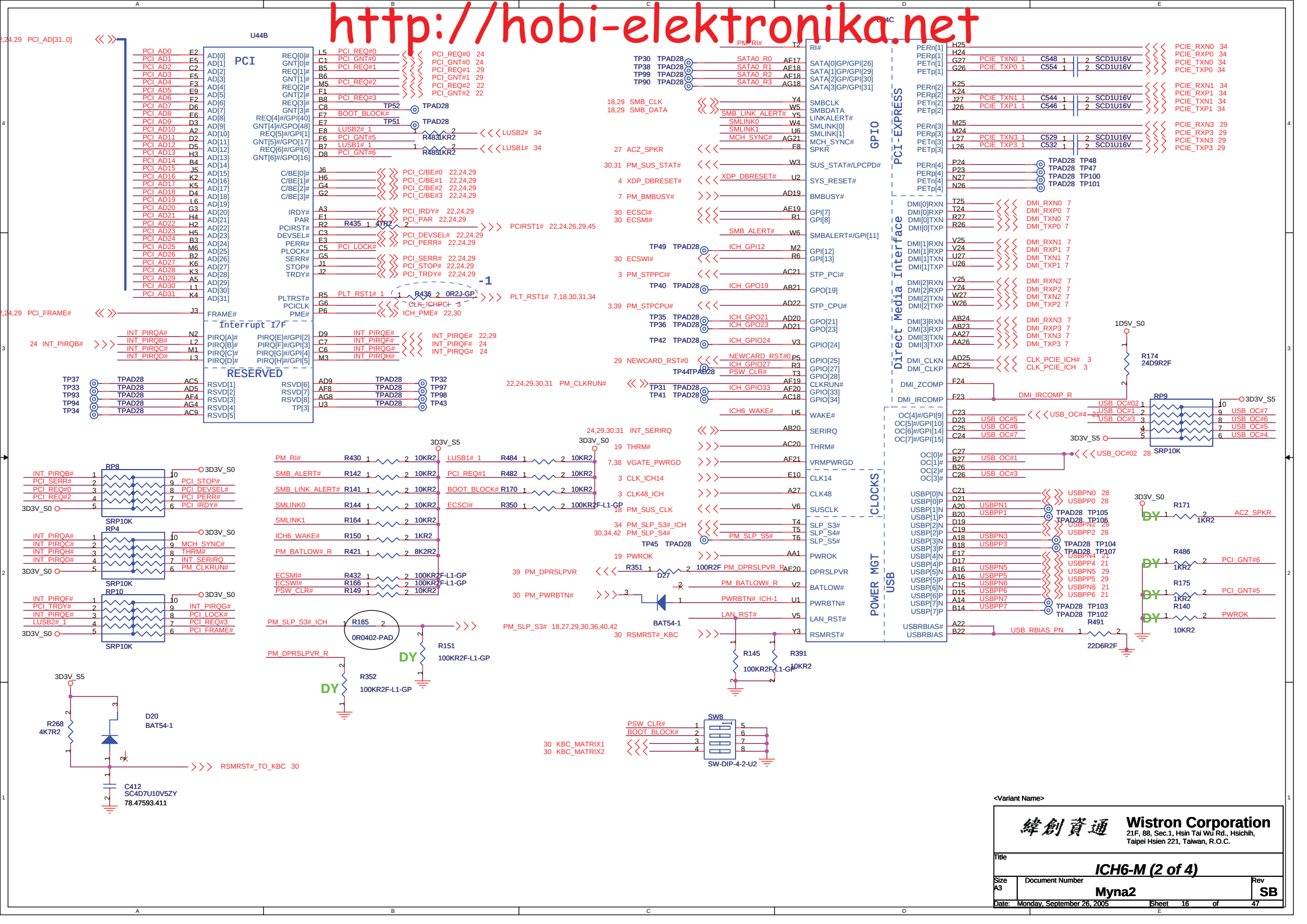
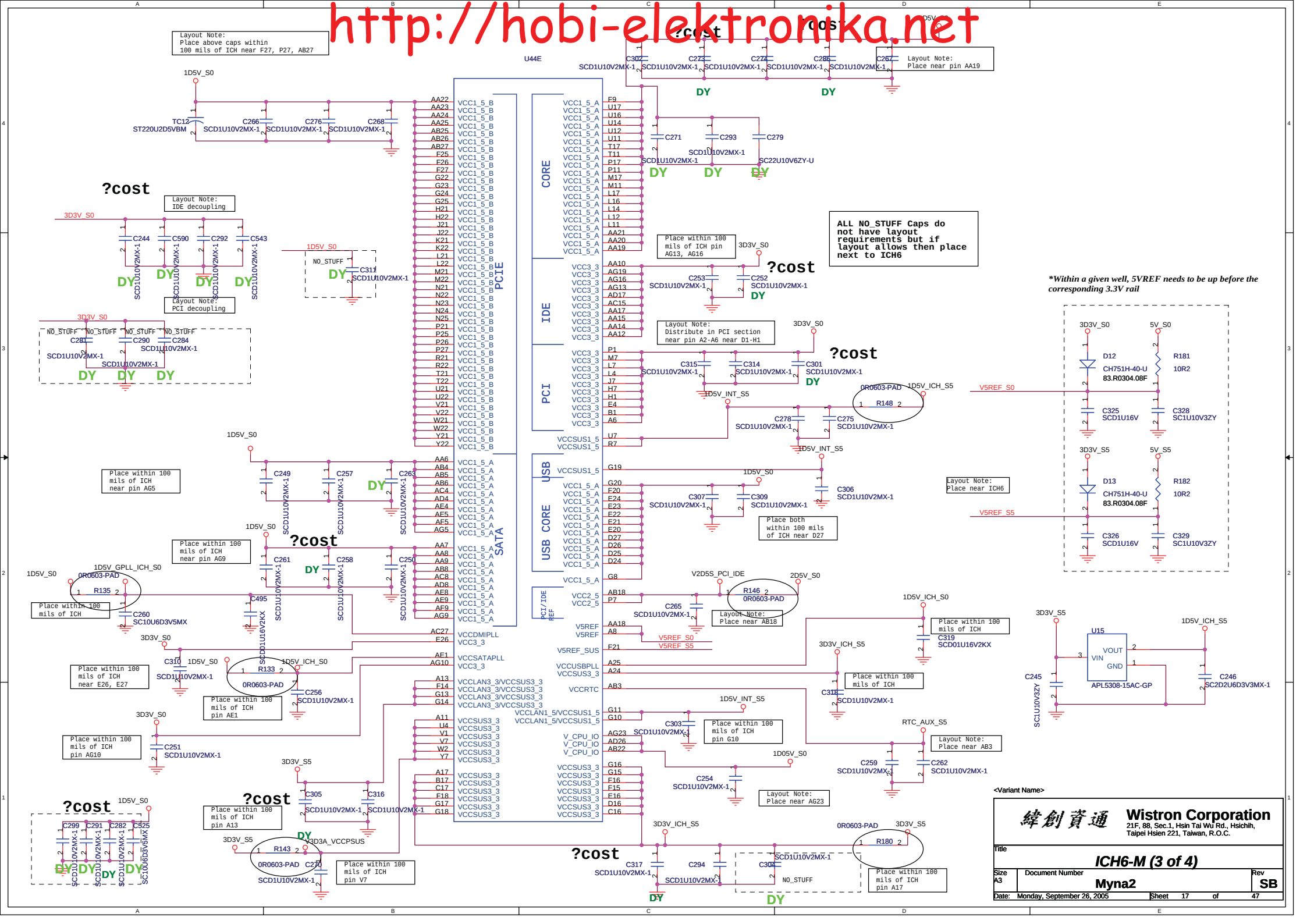
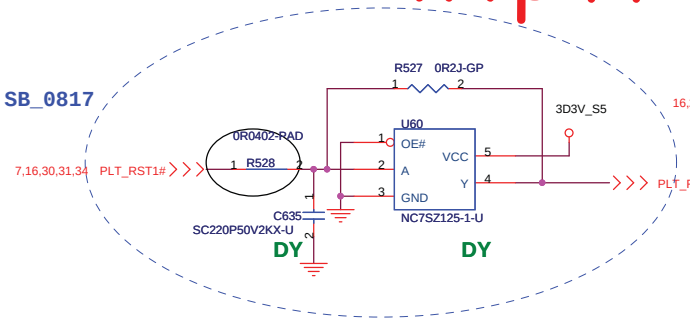
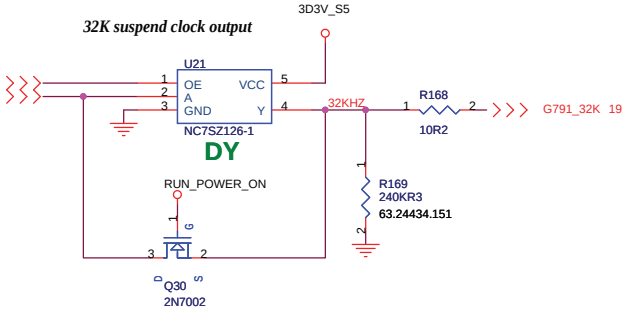
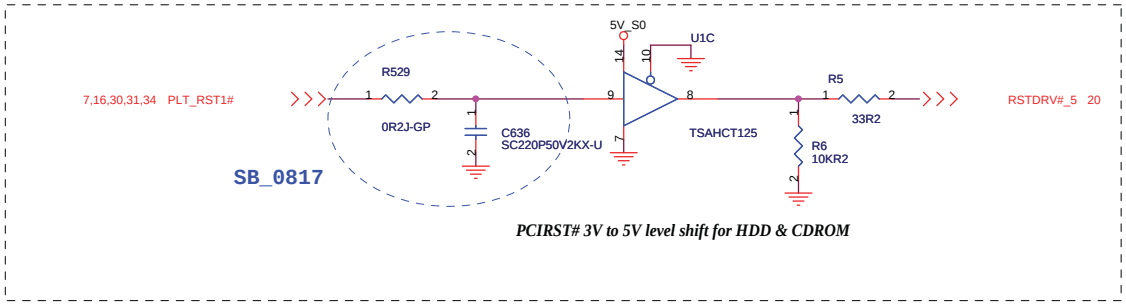


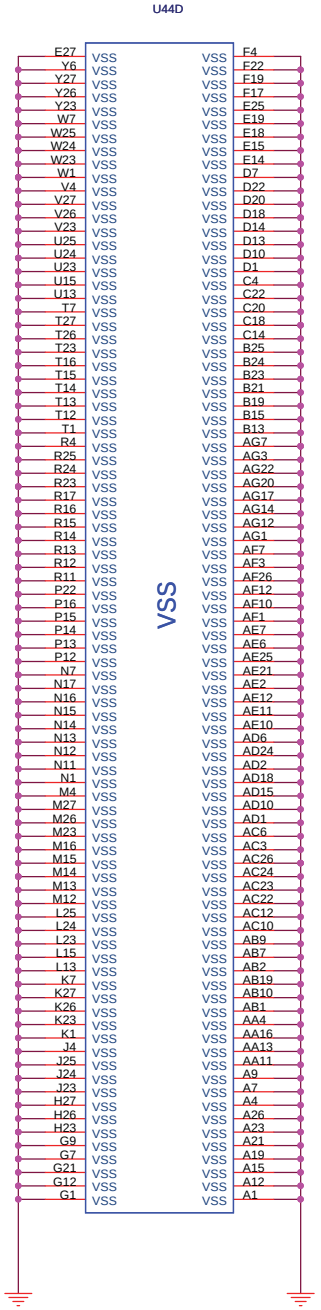




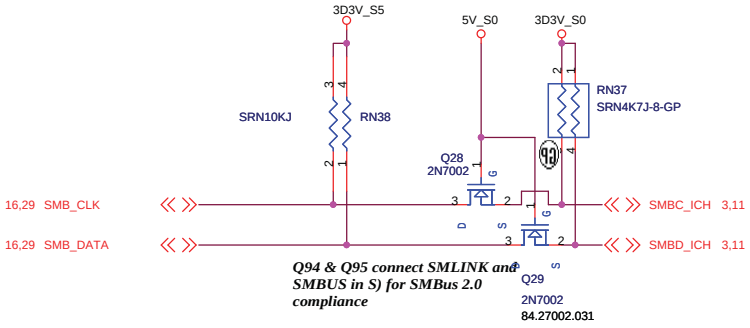








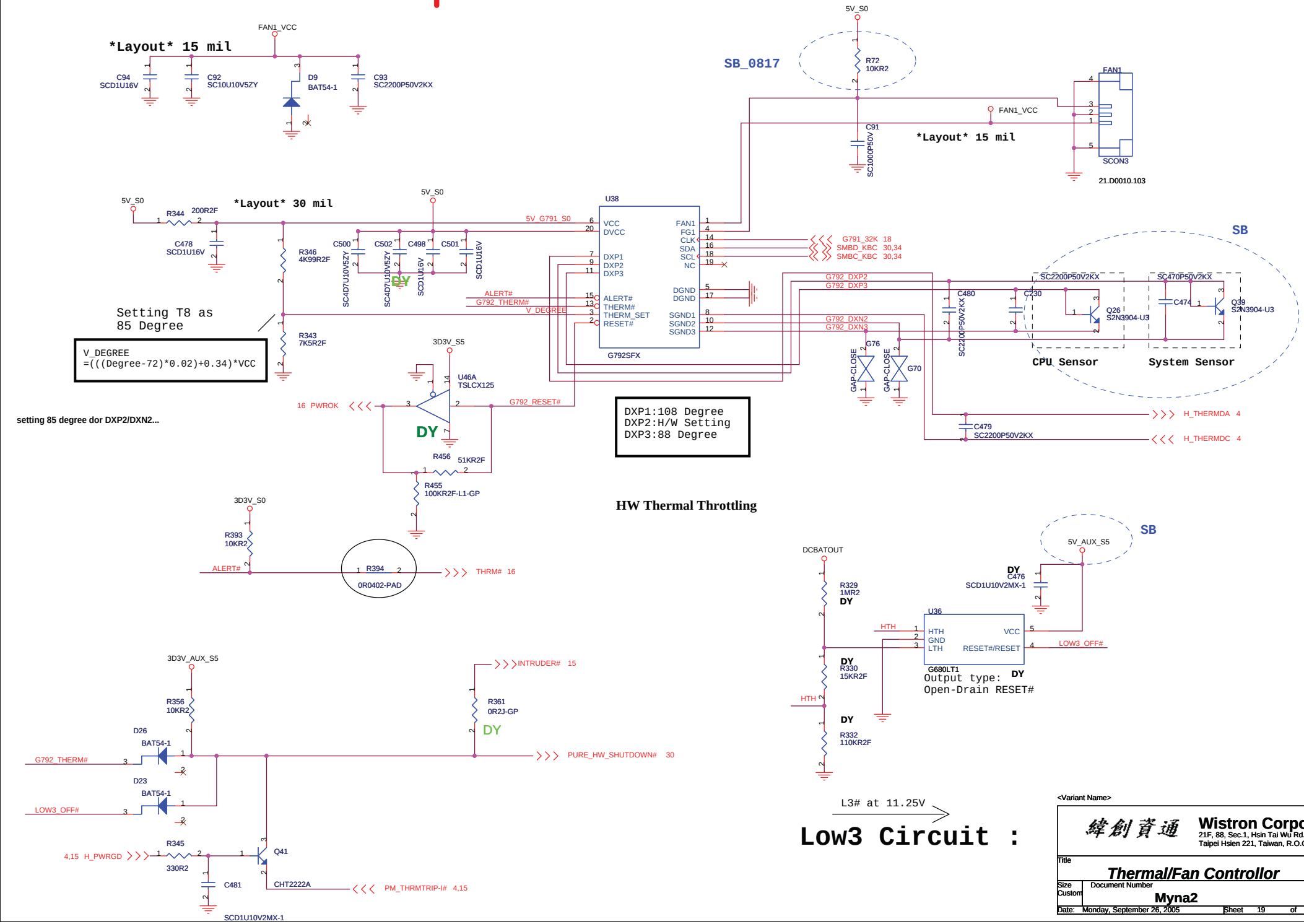
SMBUS



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

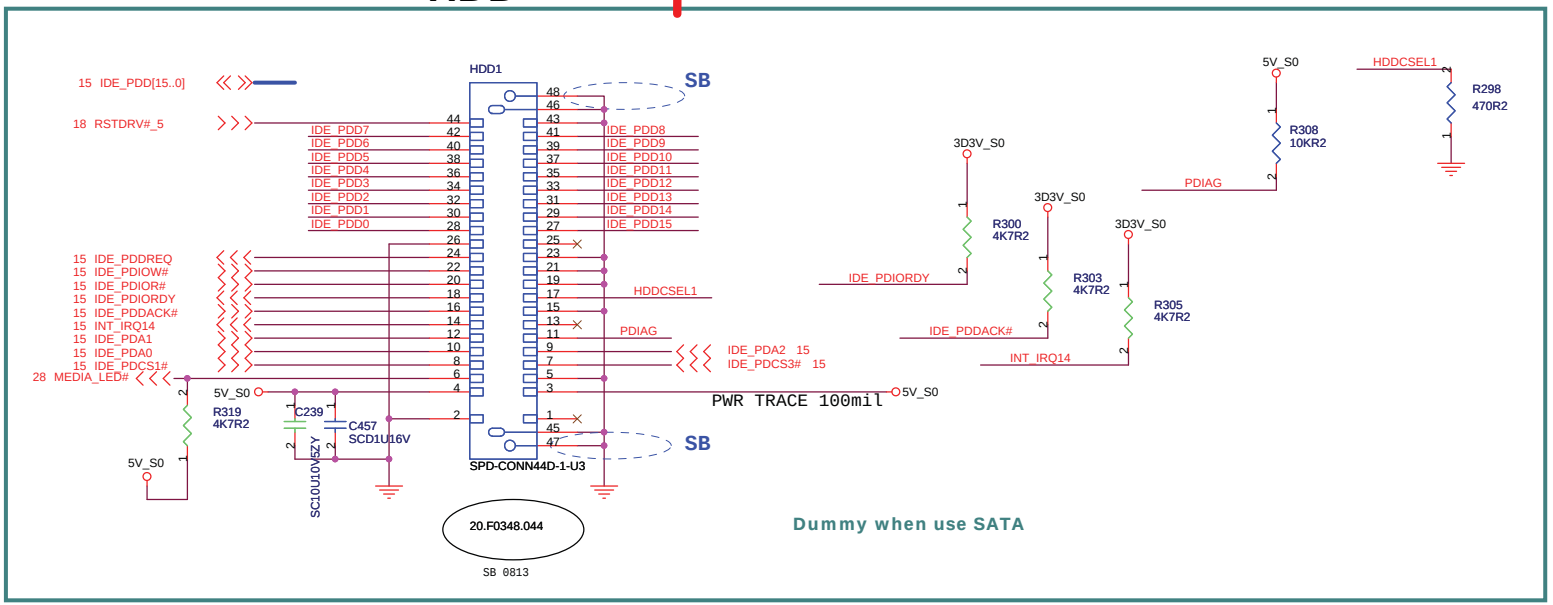
Title	ICH6-M (4 of 4)	
Size A3	Document Number Myna2	Rev SB
Date: Monday, September 26, 2005	Sheet 18 of 47	



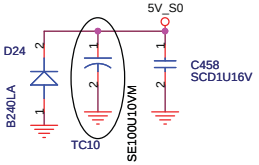
<Variant Name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Thermal/Fan Controllor
Size: Custom	Document Number: Myna2 — Rev: SB
Date: Monday, September 26, 2005	Sheet 19 of 47

HDD



For HDD & SATA both



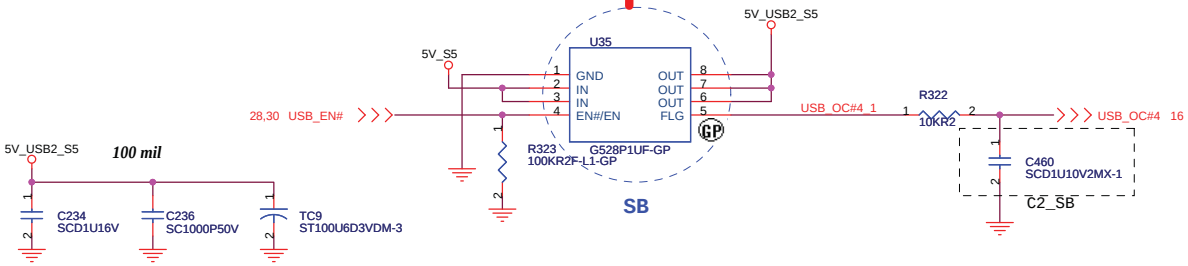
79.10711.4C1

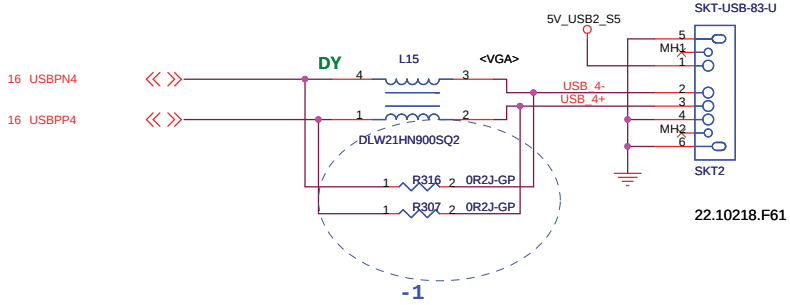
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

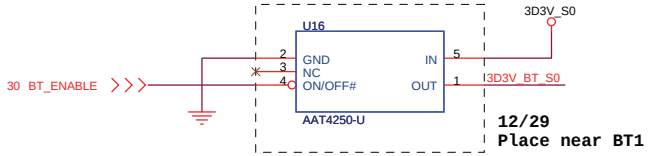
Title: PATA / SATA-HDD		
Size: A3	Document Number: Myna2	Rev: SB
Date: Monday, September 26, 2005	Sheet 20 of 47	

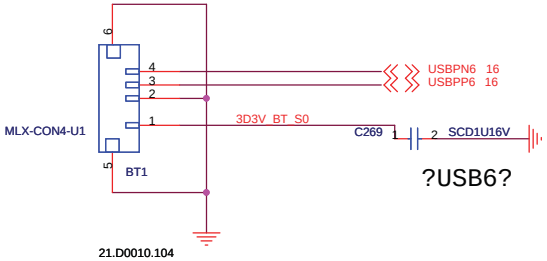
USB PORT





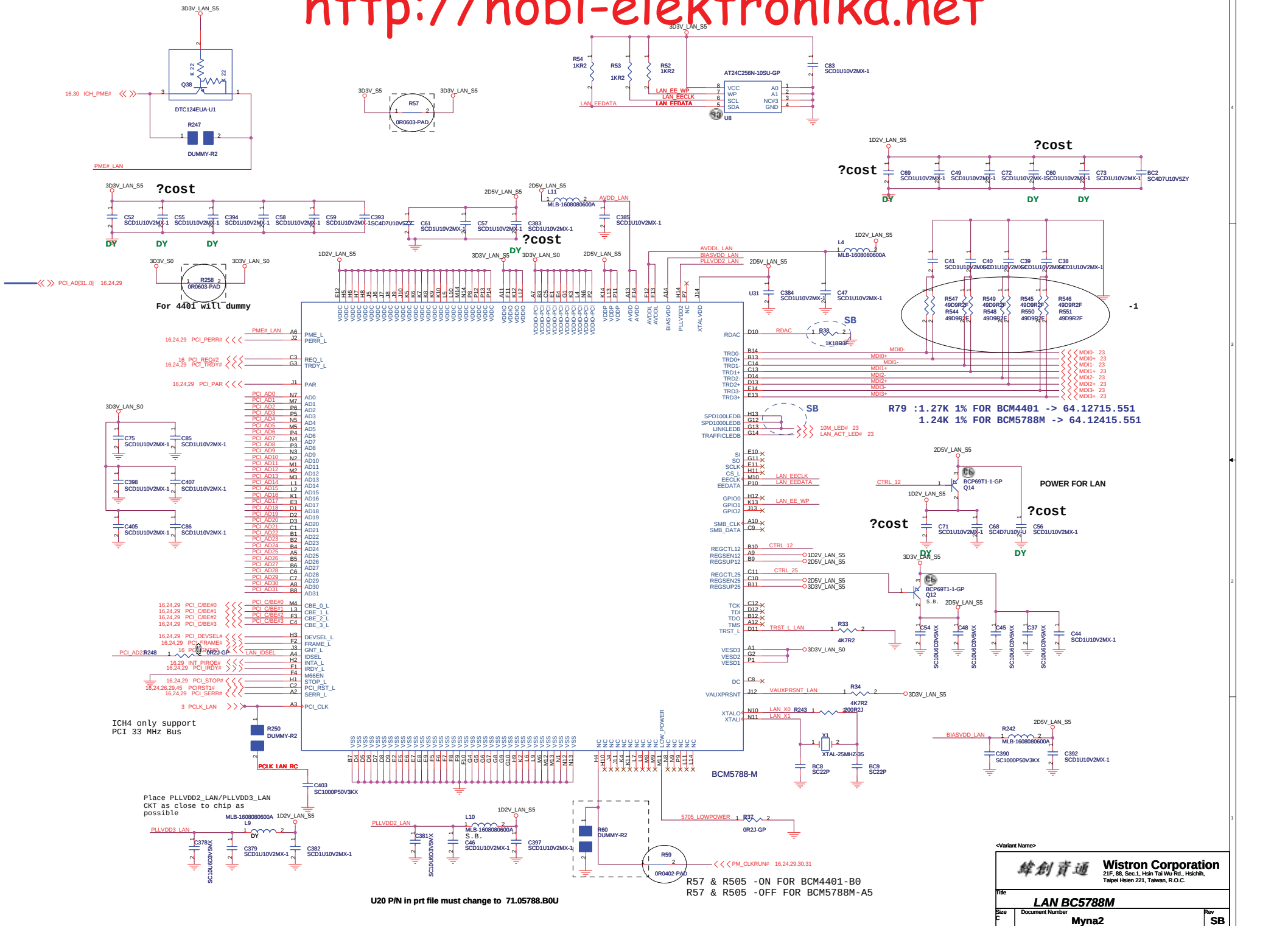
BLUETOOTH MODULE CONNECTOR





<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB & MDC & BTOOTH		
Size: A3	Document Number: Myna2	Rev: SB
Date: Monday, September 26, 2005	Sheet 21 of 47	

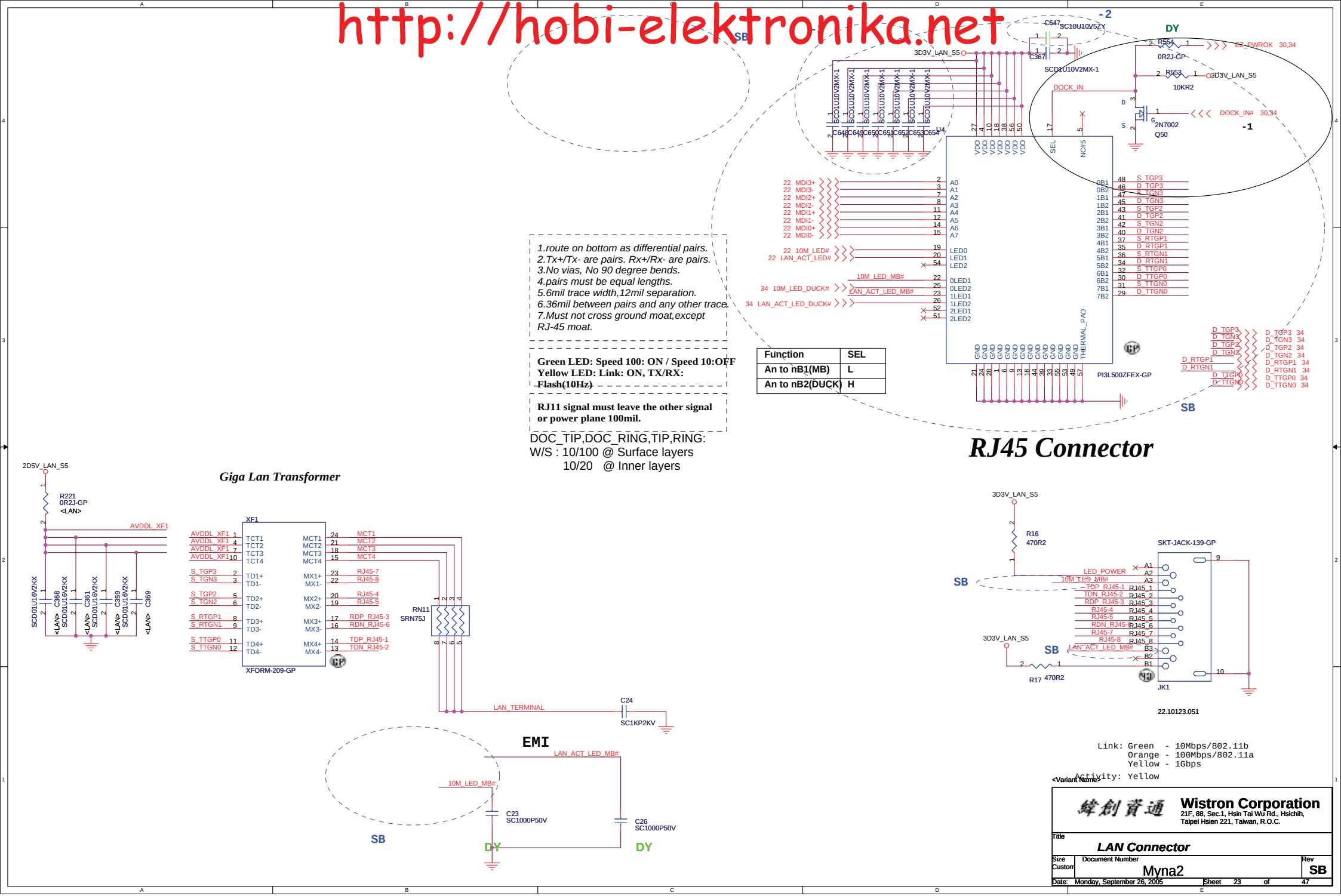


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

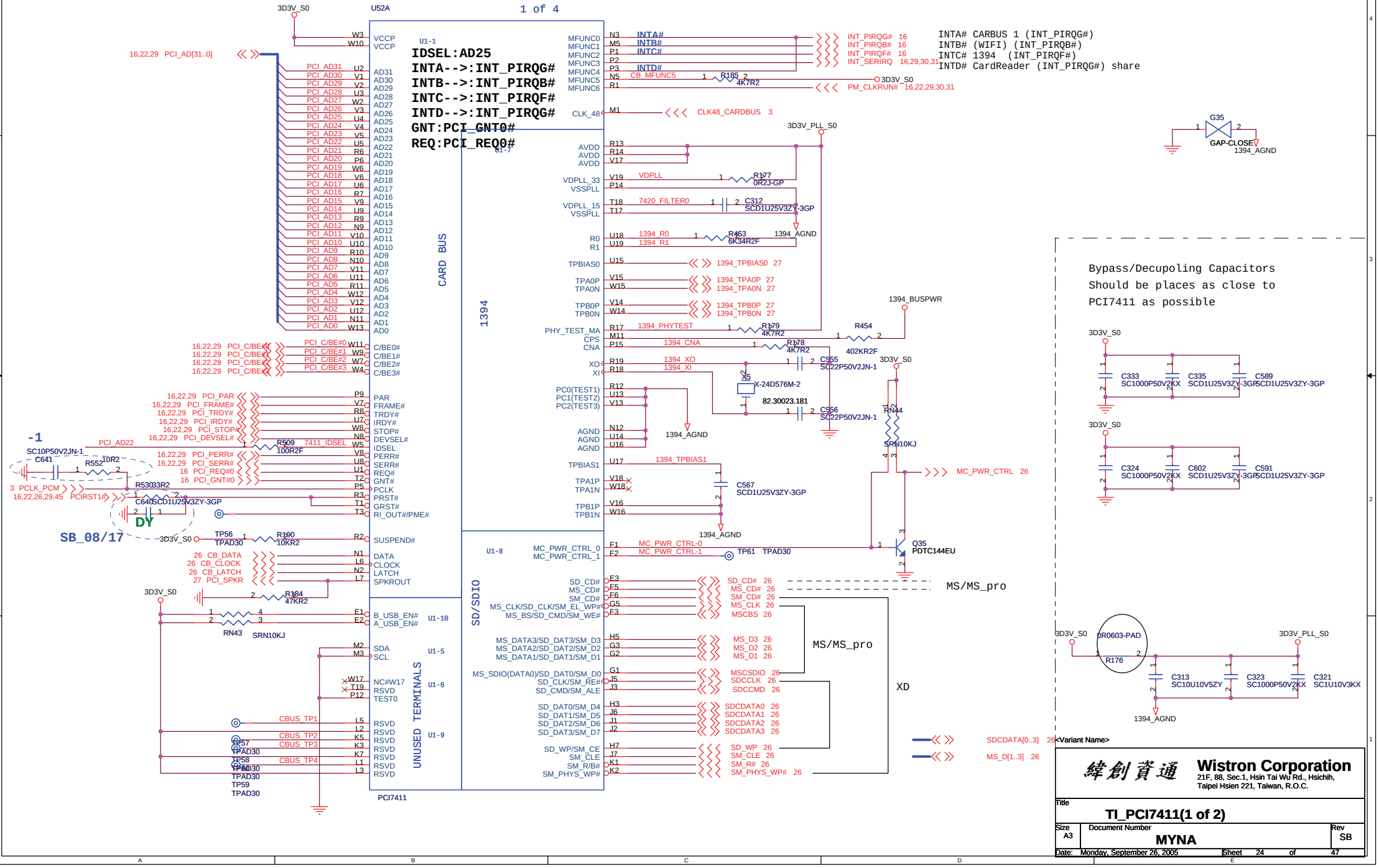
Title: LAN BC5788M

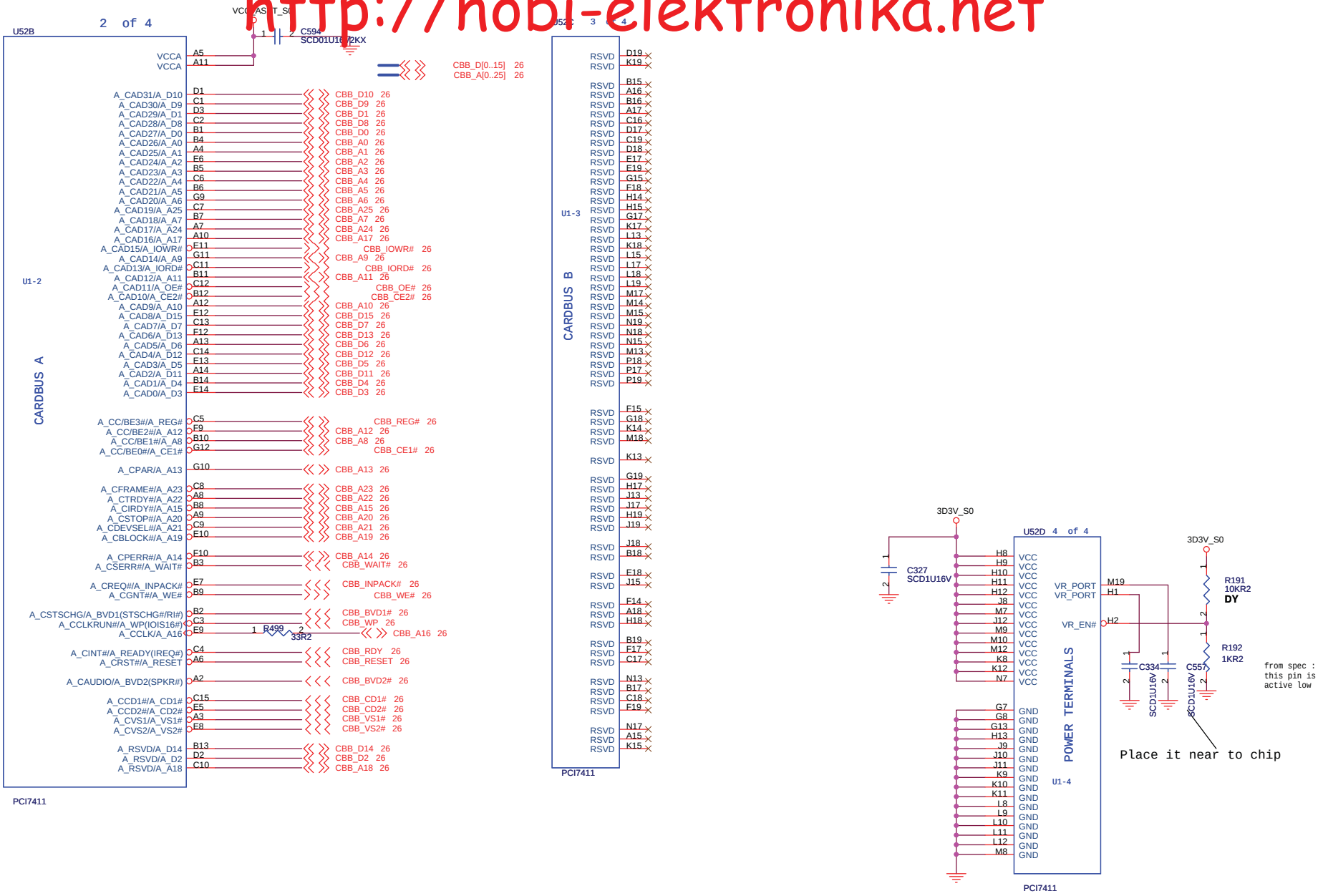
Size	Document Number	Rev
C	Myna2	SB

Date: Monday, September 26, 2005 Sheet 22 of 47



鋒創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	LAN Connector		
Size: Custom	Document Number: Myna2		Rev: SB
Date: Monday, September 26, 2005	Sheet 23 of 47		





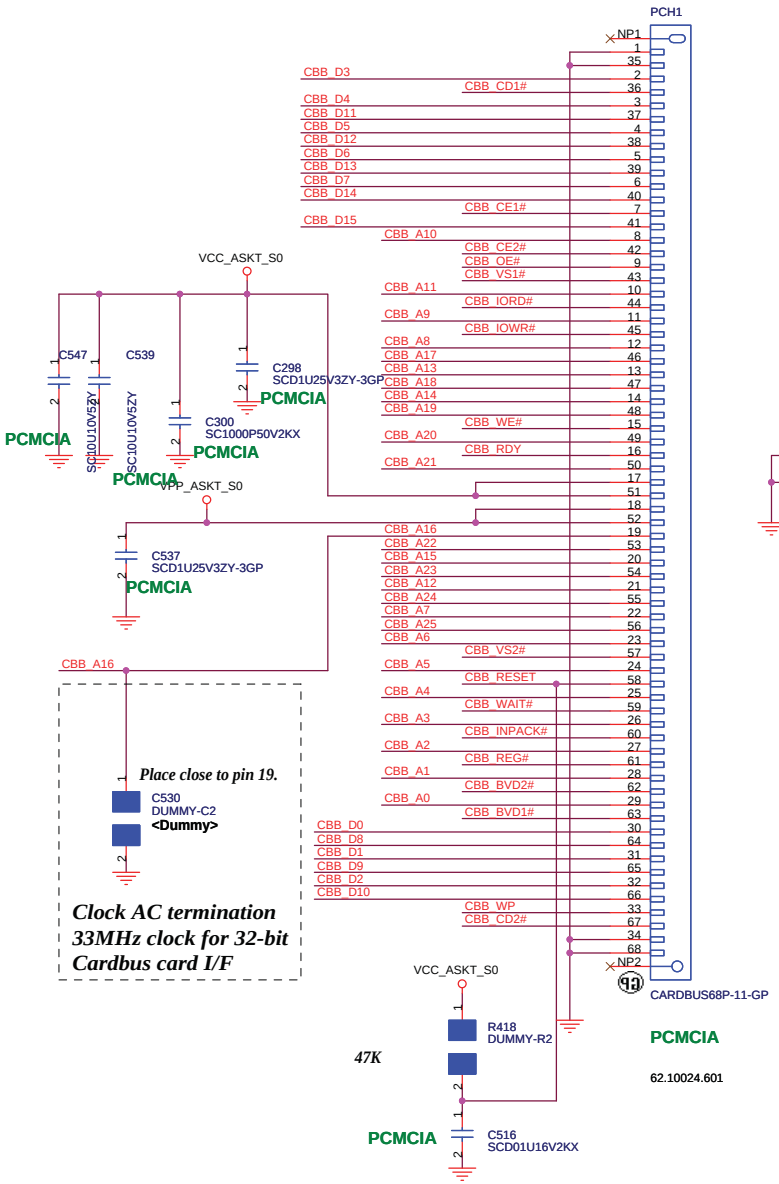
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

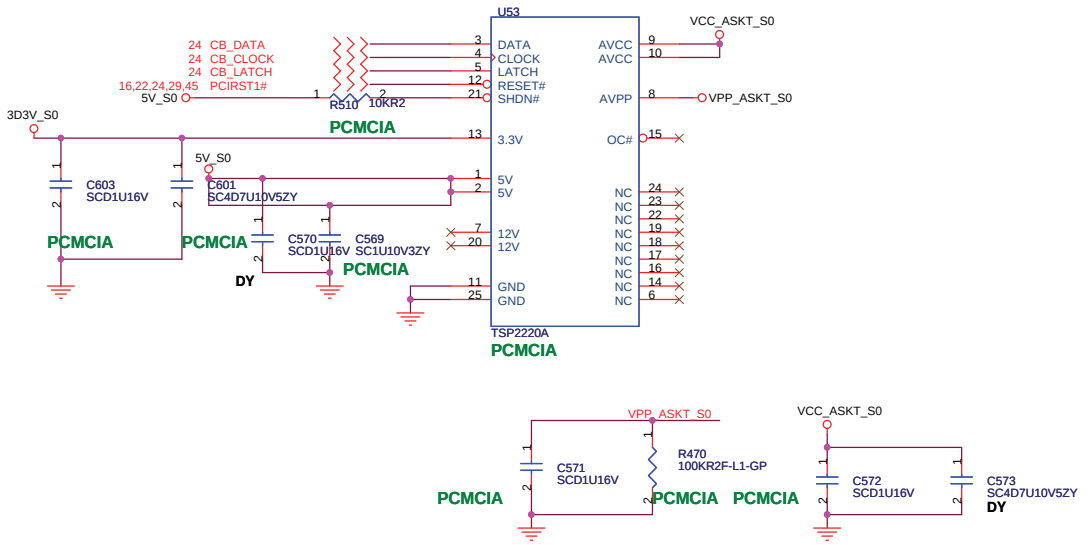
Title	TI_PCI7411(2 of 2)	
Size A3	Document Number MYNA	Rev SB
Date: Monday, September 26, 2005	Sheet 25 of 47	

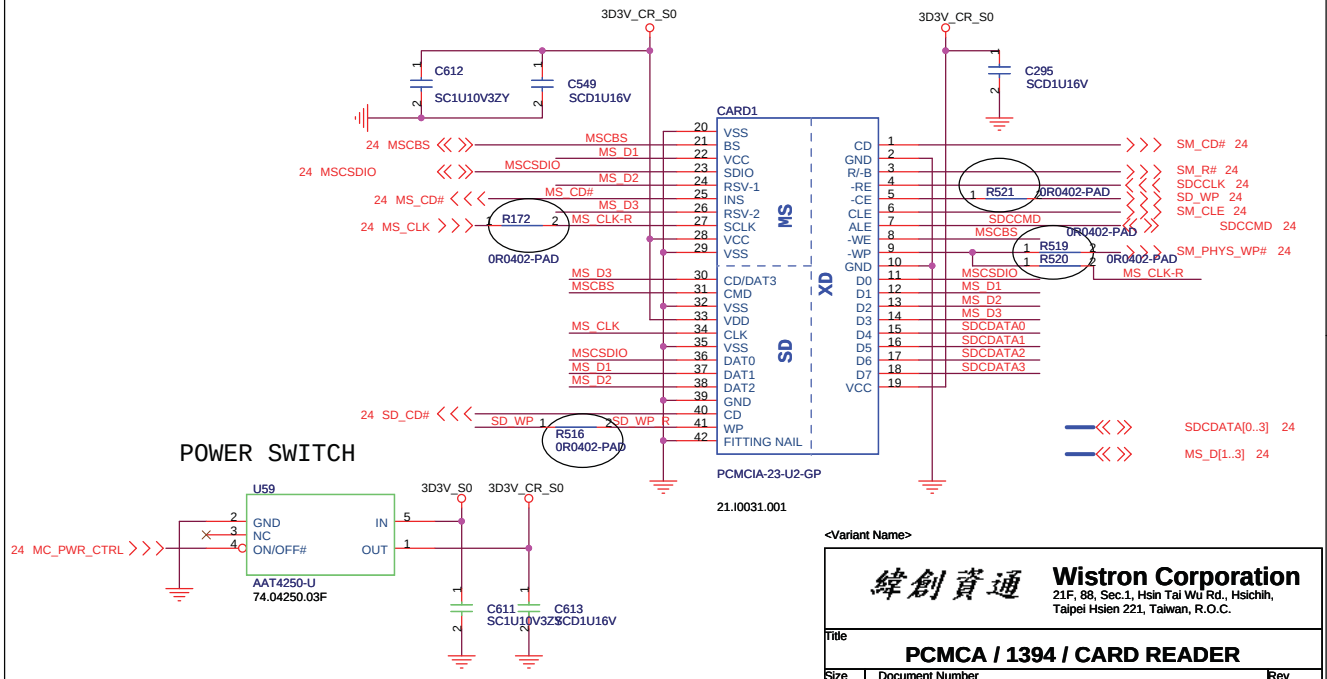
PCMCIA Socket

Cardbus I/F



Power switch



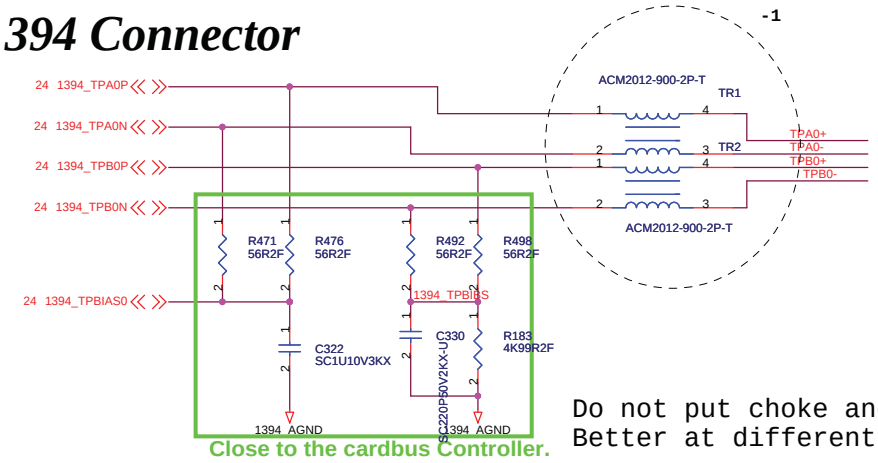


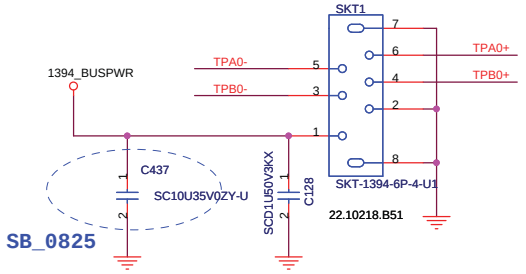
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCMCA / 1394 / CARD READER	
Size A3	Document Number Myna2	Rev SB
Date: Monday, September 26, 2005	Sheet 26 of 47	

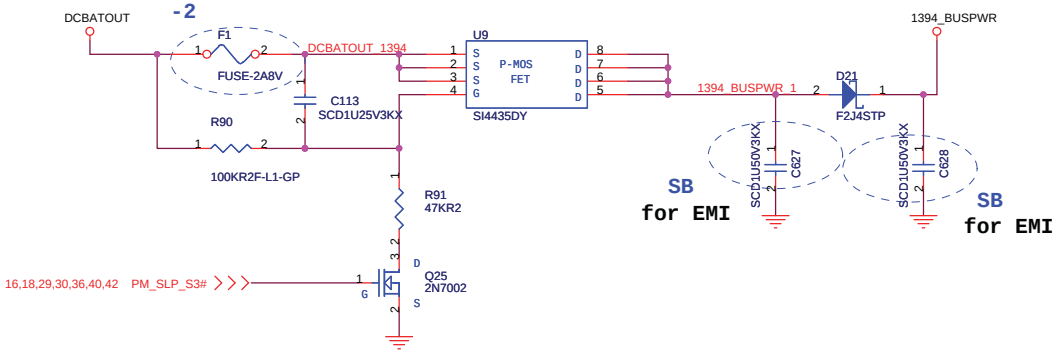
1394 Connector

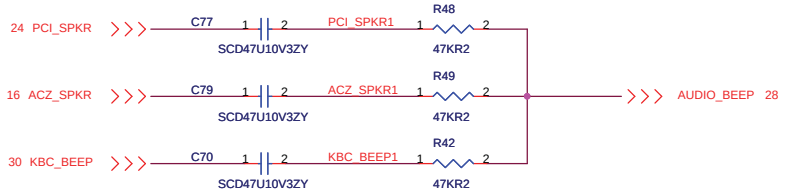




Do not put choke and 0 ohm at same location.
Better at different side.

4/21 External ODD will suck more than 1.5A when battery mode



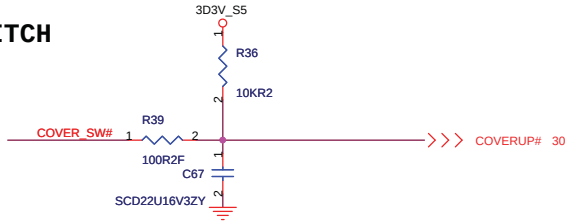


<Variant Name>

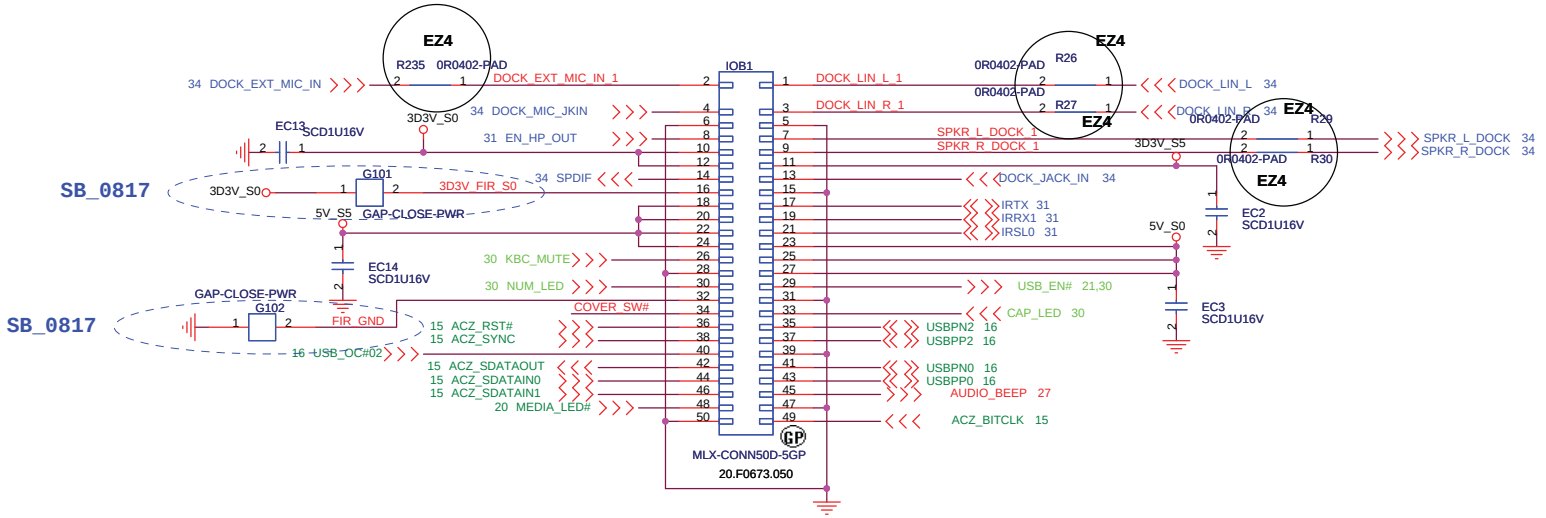
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1394 Connector		
Size: A3	Document Number: Myna2	Rev: SB
Date: Monday, September 26, 2005	Sheet 27 of 47	

COVER SWITCH



IO BD CONN.



Blue -> Dock or SuperIO
Light Green -> KBC
Green -> SouthBridge

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AC'97 CODEC - ALC655	
Size A3	Document Number Myna2	Rev SB
Date: Monday, September 26, 2005	Sheet 28 of 47	

IDSEL:AD21
INTA-->:INT_PIRQE#
GNT:PCI_GNT1#
REQ:PCI_REQ1#

PIN 3-16 : LAN RESERVE

MINI1
PCIMODEM124A1U1
62.10032.001

Geometry : 102003-6
CARDBUS-SKT61-UGP
21.H0096.001
For Newcard socket

JAE-CON26-1-GP
20.F0559.026

SB_0817
del R474

NEWCARD Connector

Reserve the symbol
for bottom side
connector

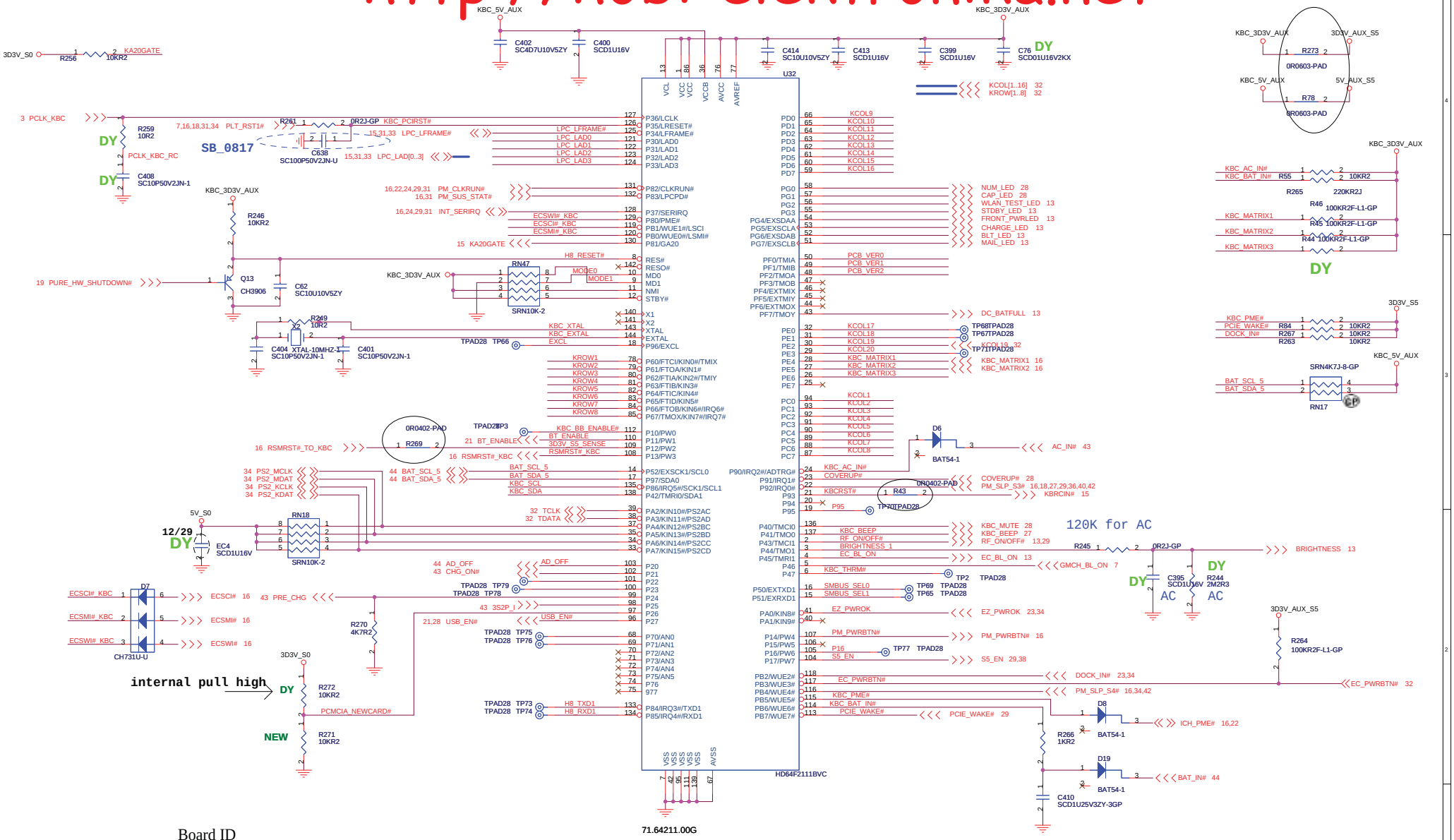
U56
TPS2231RGP-GP

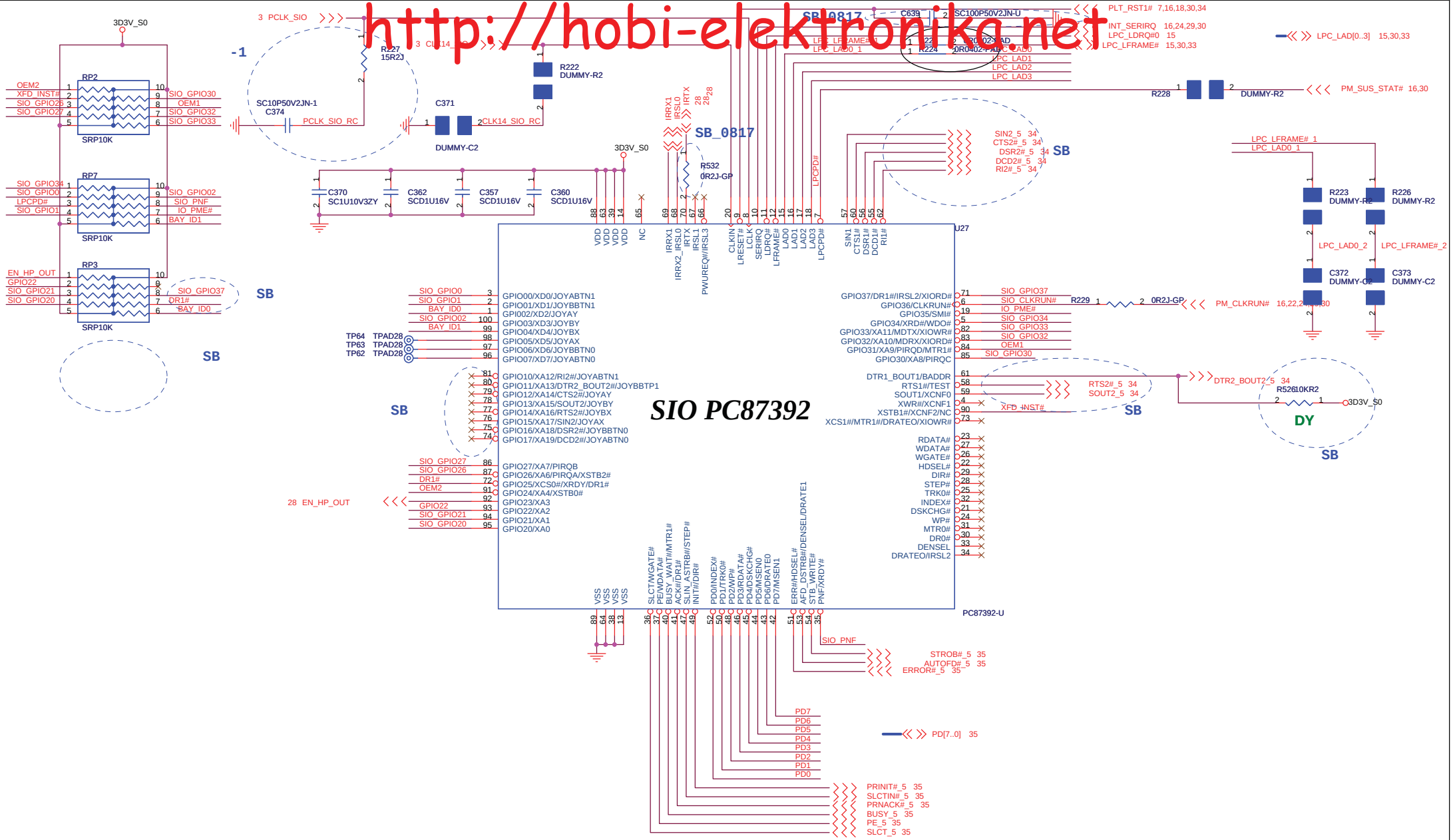
Place them Near to Chip

Place them Near to Connector

<Variant Name>

Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI-PCI/NEW Card		
Size: A3	Document Number: Myna2	Rev: SB
Date: Monday, September 26, 2005	Sheet 29 of 47	

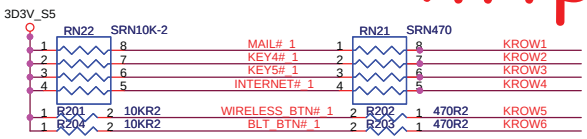




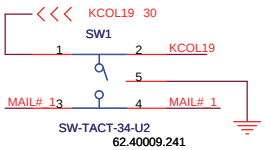
<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SIO		
Size: A3	Document Number: Myna2	Rev: SB
Date: Monday, September 26, 2005	Sheet 31 of 47	

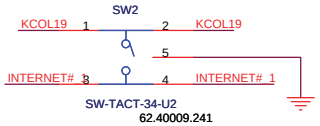
Launch BD CONN



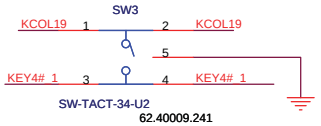
MAIL BUTTON



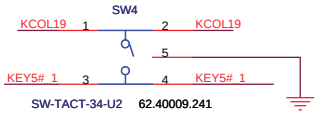
INTERNET BUTTON

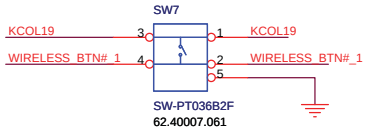


P4 BUTTON

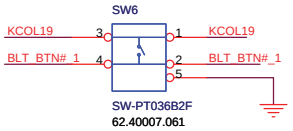


P5 BUTTON

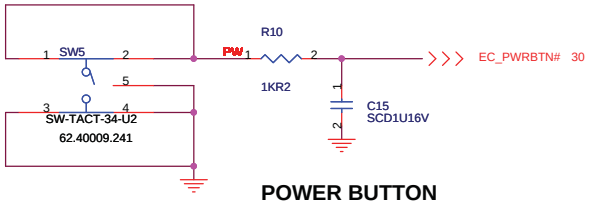




WIRELESS BUTTON

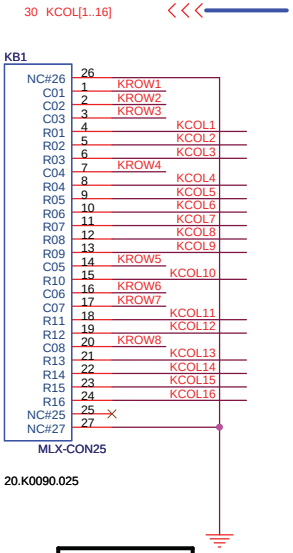


BLUETOOTH BUTTON

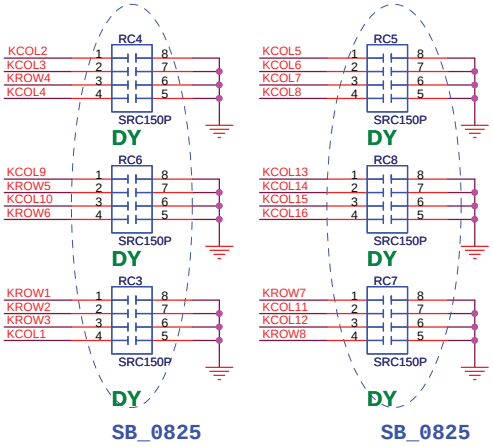


POWER BUTTON

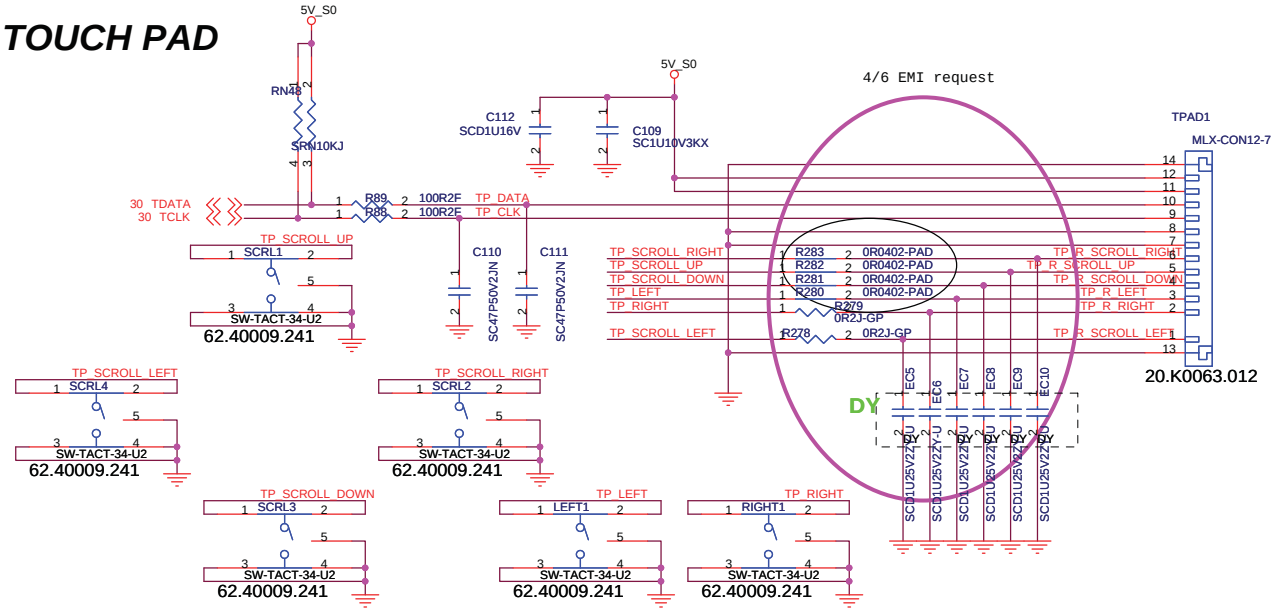
Internal KeyBoard Connector



EMI CAPS



TOUCH PAD



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **KBC&TPAD CONN**		
Size: A3	Document Number: **Myna2**	Rev: **SB**
Date: Monday, September 26, 2005	Sheet 32 of 47	

? if use Debug Board, remove this R

Unused FGPI pins must not be float

SB_0817

PLT_RST1_2# — R195 100R2F — FWHRST#

C643 SC150P50V2JN

-1

RP11 SRP10K 66.10336.100

SELECT_FWH, FWH_FGPI4, FWH_FGPI3, FWH_FGPI2, FWH_FGPI1, FWH_FGPI0

15,30,31 LPC_LAD[0:3]

TOP VIEW

A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)

(BOTTOM VIEW)

FLASH ROM

512K Bits X 8 = 4M Bits

3D3V_S0

C341 SCD1U16V

C340 SC1U10V3ZY

U58

NC, NC, NC, VSS, IC, A10/FGPI4, R/C#(CLK), VDD, NC, RST#, A9(FGPI3), A8(FGPI2), A7(FGPI1), A6(FGPI0), A5(WP#), A4(TBL#)

OE#/INIT#, WE#/FWH4, NC, DQ7/RES, DQ6/RES, DQ5/RES, DQ4/RES, DQ3/LAD3, VSS, DQ2/LAD2, DQ1/LAD1, DQ0/LAD0, A0/ID0, A1/ID1, A2/ID2, A3/ID3

FWH_INIT#, LPC_LFRAME#, LPC_LAD3, LPC_LAD2, LPC_LAD1, LPC_LAD0

SELECT_FWH, FWH_FGPI4, PCLK_FWH, FWHRST#, FWH_FGPI3, FWH_FGPI2, FWH_FGPI1, FWH_FGPI0

BC15 DUMMY-C3, R515 DUMMY-R3

R522 10KR2 — 3D3V_S0

49LF004A-33

SECOND SOURCE
72.39040.H09

GOLDEN FINGER FOR DEBUG BOARD

SB_0817

18,29 PLT_RST1_2#
15,30,31 LPC_LFRAME#
3 PCLK_FWH
15 FWH_INIT#

5V_S0

U23

A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15

B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15

PLT_RST1_2#, LPC_LFRAME#, PCLK_FWH, FWH_INIT#, LPC_LAD3, LPC_LAD2, LPC_LAD1, LPC_LAD0, EXT_FWH#

3D3V_S0

FOX-GF30
ZZ.GF030.XXX

SB_0817

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

3D3V_S0

C331 SC10U6D3V5MX

C605 SCD1U16V

C320 SCD1U16V

DY DY DY

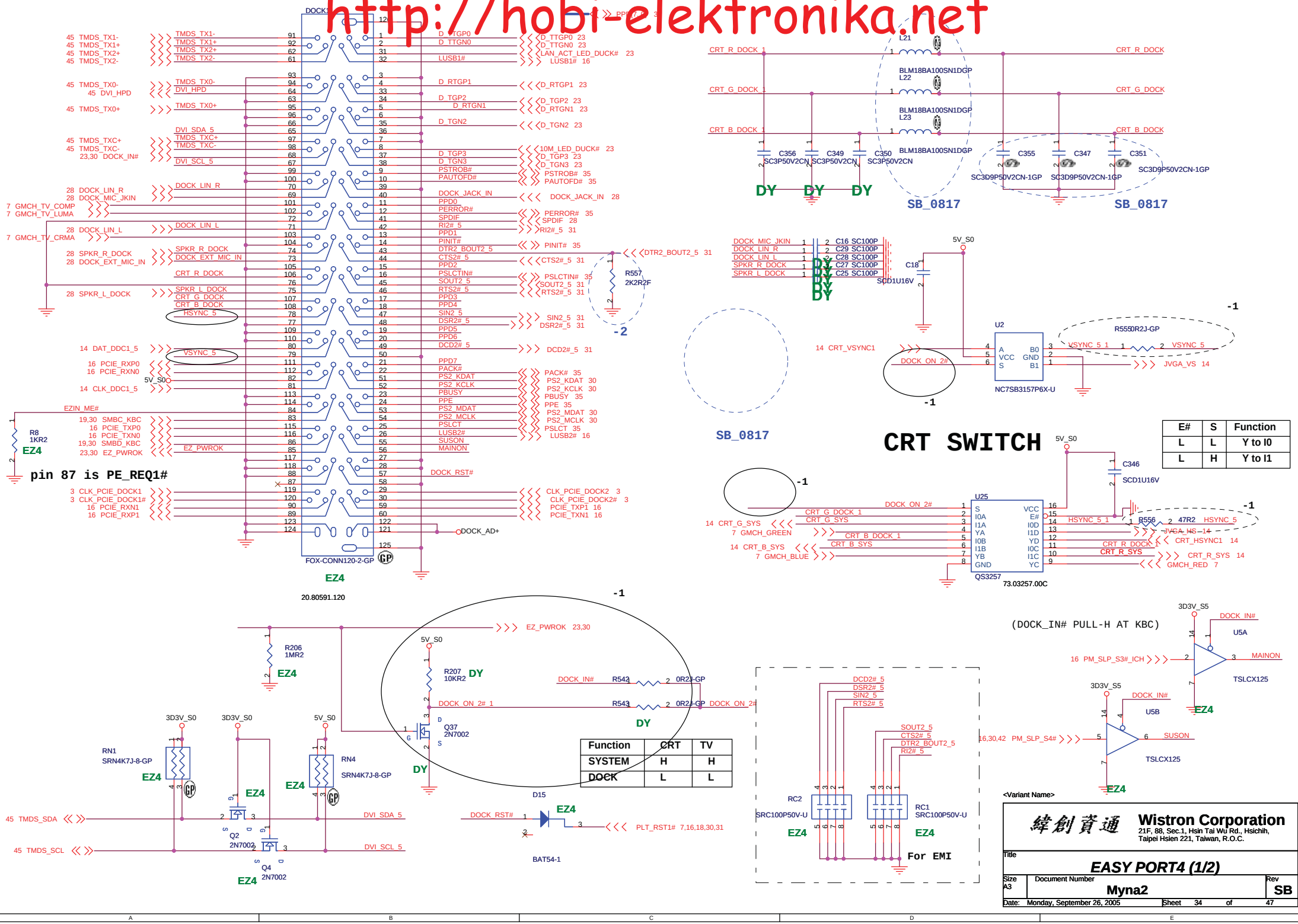
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

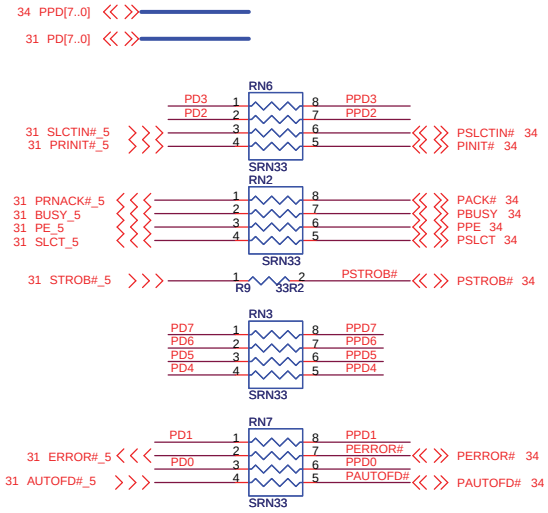
Title: FWH and Debug

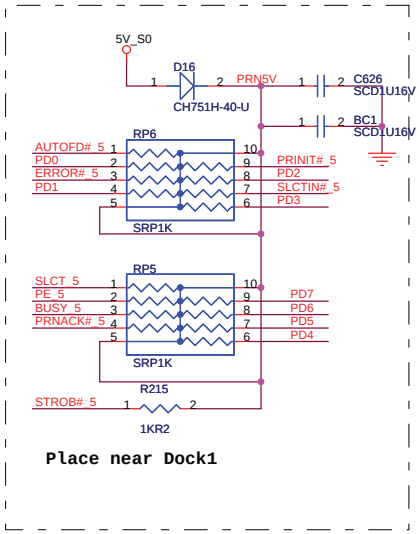
Size: A3 | Document Number: Myna2 | Rev: SB

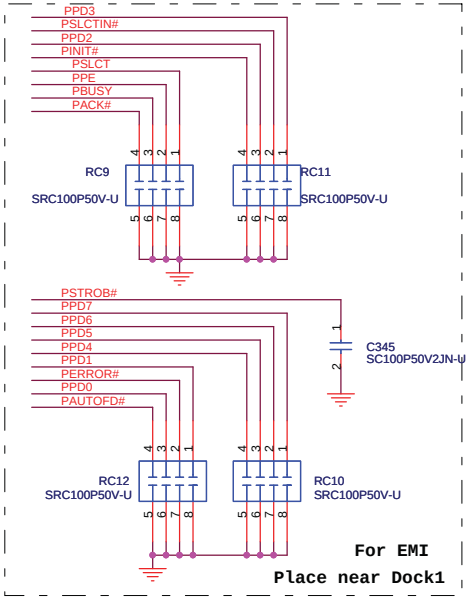
Date: Monday, September 26, 2005 | Sheet 33 of 47



PRINT PORT



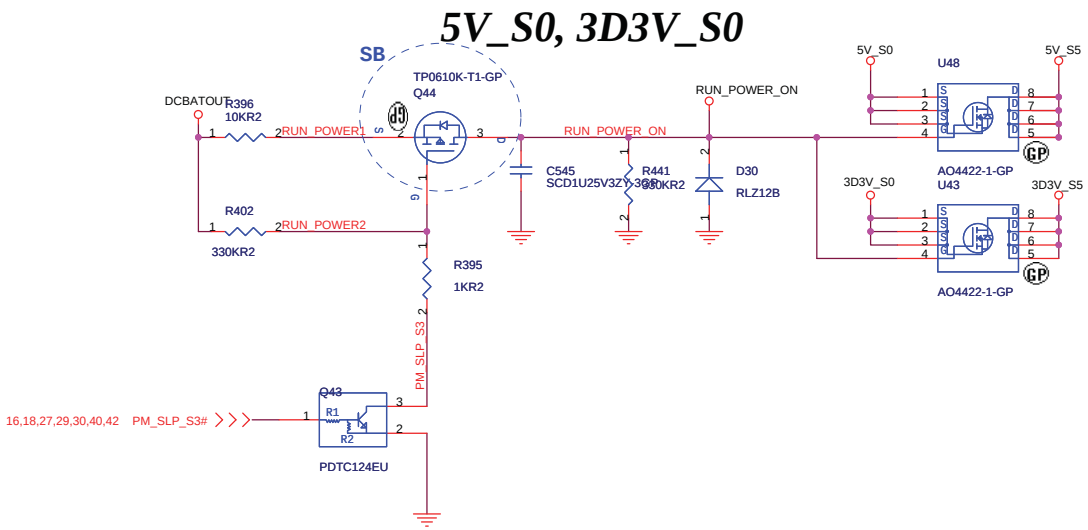




<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	EASY PORT4 (2/2)	
Size A3	Document Number Myna2	Rev SB
Date: Monday, September 26, 2005	Sheet 35 of 47	



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***RUN Power***
Size A3	Document Number **Myna2** Rev **SB**
Date: Monday, September 26, 2005	Sheet 36 of 47

CPU_CORE MAX1907AETL-U

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5

VID Setting
VID0(I / 1.05V)
VID1(I / 1.05V)
VID2(I / 1.05V)
VID3(I / 1.05V)
VID4(I / 1.05V)
VID5(I / 1.05V)

Output Signal
PGOOD(OD / 3.3V) → 1907_PGOOD
CLKEN#(OD / 0V) → VVT_PWRGD#

Output Power
VCC_CORE_S0(O) → VCC_CORE_S0 (27A)

CPUCORE_ON
PM_DPRSLPVR
PM_STPCPU#

Input Signal
SHDN#(I / 3.3V)
SUS(I / 3.3V)
DPSLP# (I / 3.3V)

DCBATOUT
5V_S5

Input Power
VCC
VDD

TPS5130 3D3V/5V/1D05V/2D5V

SHUTDOWN_S5
SHUTDOWN_S5
PM_SLP_S3#
PM_SLP_S3#
DCBATOUT_5130
DCBATOUT_5130

Input Signal
SS_STBY1(I / 5V) FOR 3.3V
SS_STBY2(I / 5V) FOR 5V
SS_STBY3(I / 5V) FOR 1.05V
STBY_LDO(I / 5V) FOR 2.5V
STBY_VREF5(I / 28V)
STBY_VREF3.3(I / 28V)

DCBATOUT
5V_S5
5V_AUX_S5
3.3V_S0

Input Power
VIN (I / 28V)
REG5V_IN(I / 5V)
5V_AUX_S5
For PGOUT

Output Signal
PGOUT(OD / 5V) → CPUCORE_ON

Output Power
3D3(O) → 3D3V (5A)
5V(O) → 5V (6A)
1D05V(O) → 1D05V (6A)
2D5V (O) → 2D5V (1A)

MAX8743 1D8V/1D5V

PM_SLP_S4#
PM_SLP_S3#

Input Signal
EN1 (I)
EN2 (I)

Output Signal
PGOOD → CPUCORE_ON

5V_S5

Input Power
VCC (I)

Output Power
1D8V (O) → 1D8V_S3 (6A)
1D5V (O) → 1D5V_S0 (4A)

Charger ISL6225

CHGON#/OFF
BT_TH

Input Signal
EN
PKPRES

Output Signal
BATT → BT+SENSE
ACOK → AC_IN

AD+

Input Power
ACIN

Output Power
VOUT (O) → BT+
VOUT (O) → DCBATOUT

Adapter

AD_OFF

Input Signal
(I)

Output Signal
(O) → DC_IN+

AD_JK
5V_AUX_S5

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O) → AD+

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Diagram**

Size	Document Number	Rev
A3	Myna2	SB

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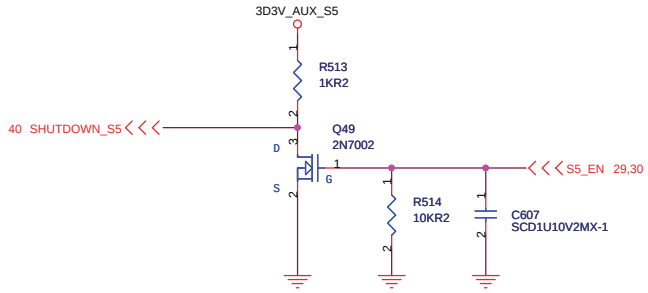

PWRGD for NB and SB

3,39 1907_PGOOD — 0R0402-PAD R147 — VGATE_PWRGD 7,16

<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***POWER ON CIRCUIT***
Size: A3	Document Number: **Myna2** — Rev: **SB**
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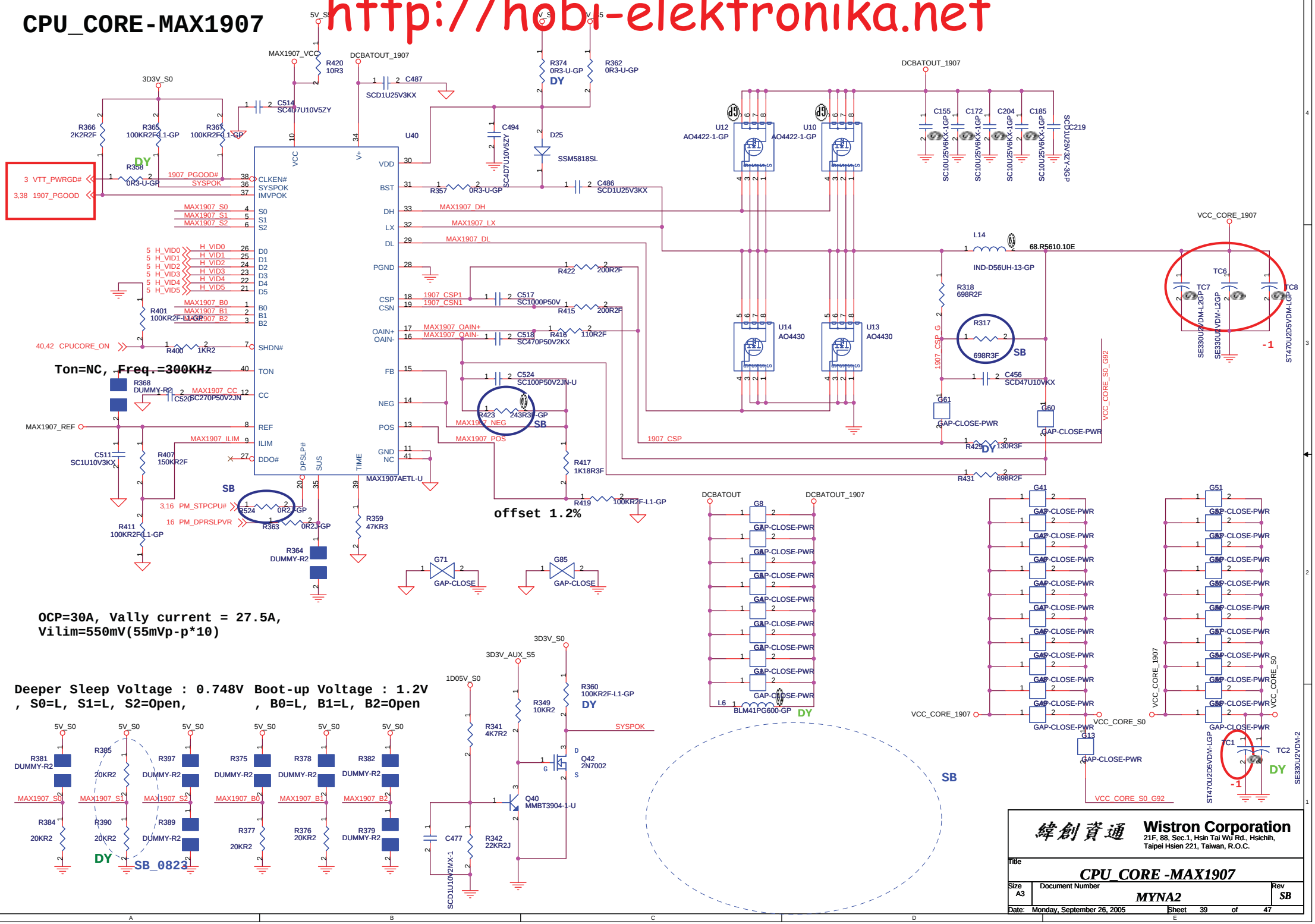
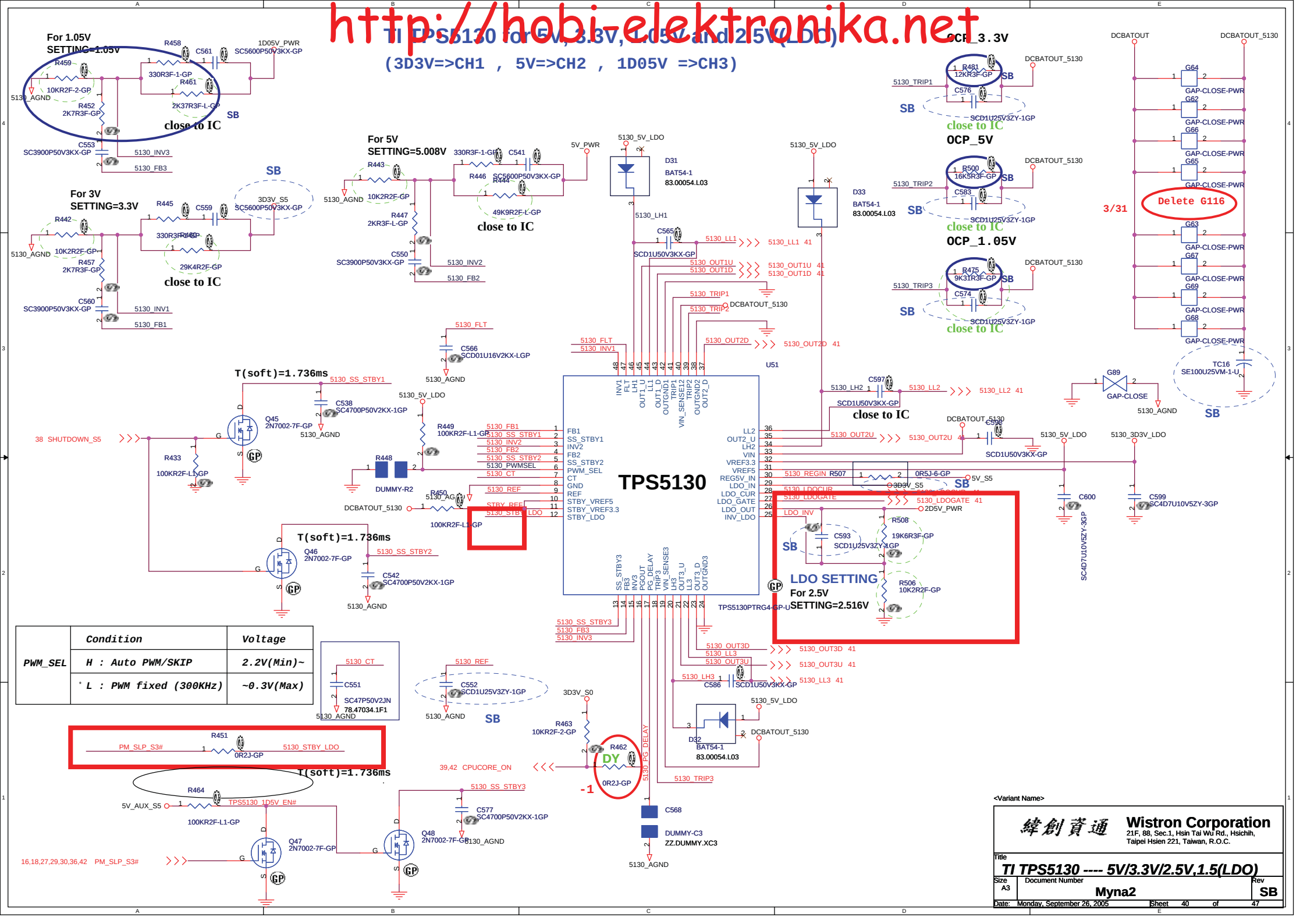
CPU_CORE-MAX1907



TI TPS5130 for 5V, 3.3V, 1.05V and 2.5V(LDO)

(3D3V=>CH1 , 5V=>CH2 , 1D05V =>CH3)



PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	L : PWM fixed (300KHz)	~0.3V(Max)

<Variant Name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	TI TPS5130 ---- 5V/3.3V/2.5V,1.5(LDO)
Size A3	Document Number: Myna2
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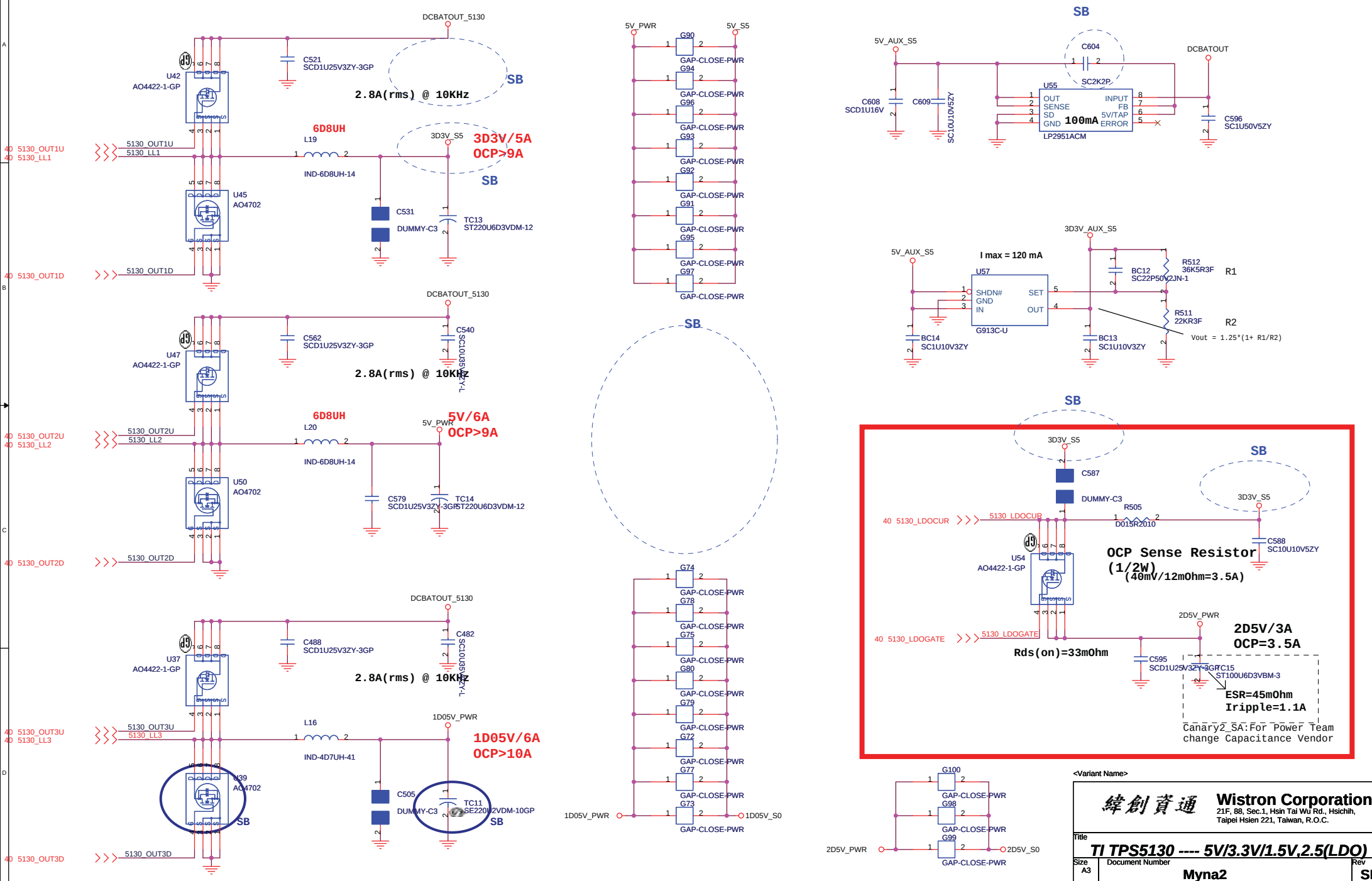
TI TPS5130 for 5V, 3.3V, 1.05V and 2.5V(LDO)

(3D3V=>CH1 , 5V=>CH2 , 1D05V =>CH3)

Aux Power



<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *TI TPS5130 ---- 5V/3.3V/1.5V,2.5(LDO)*

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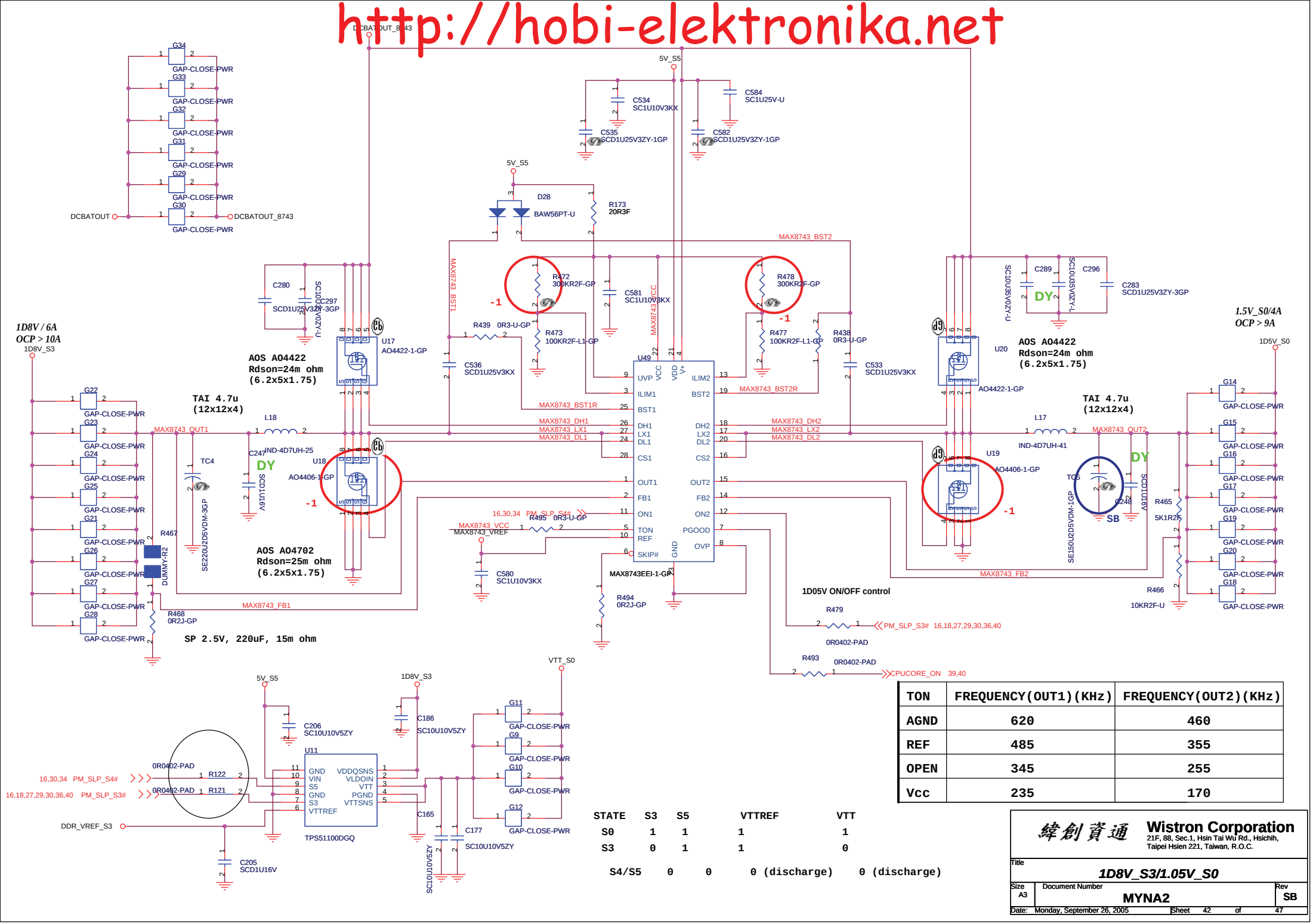

TON	FREQUENCY(OUT1)(KHz)	FREQUENCY(OUT2)(KHz)
AGND	620	460
REF	485	355
OPEN	345	255
Vcc	235	170

STATE	S3	S5	VTTREF	VTT
S0	1	1	1	1
S3	0	1	1	0
S4/S5	0	0	0 (discharge)	0 (discharge)

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D8V_S3/1.05V_S0

Size: A3 | Document Number: MYNA2 | Rev: SB

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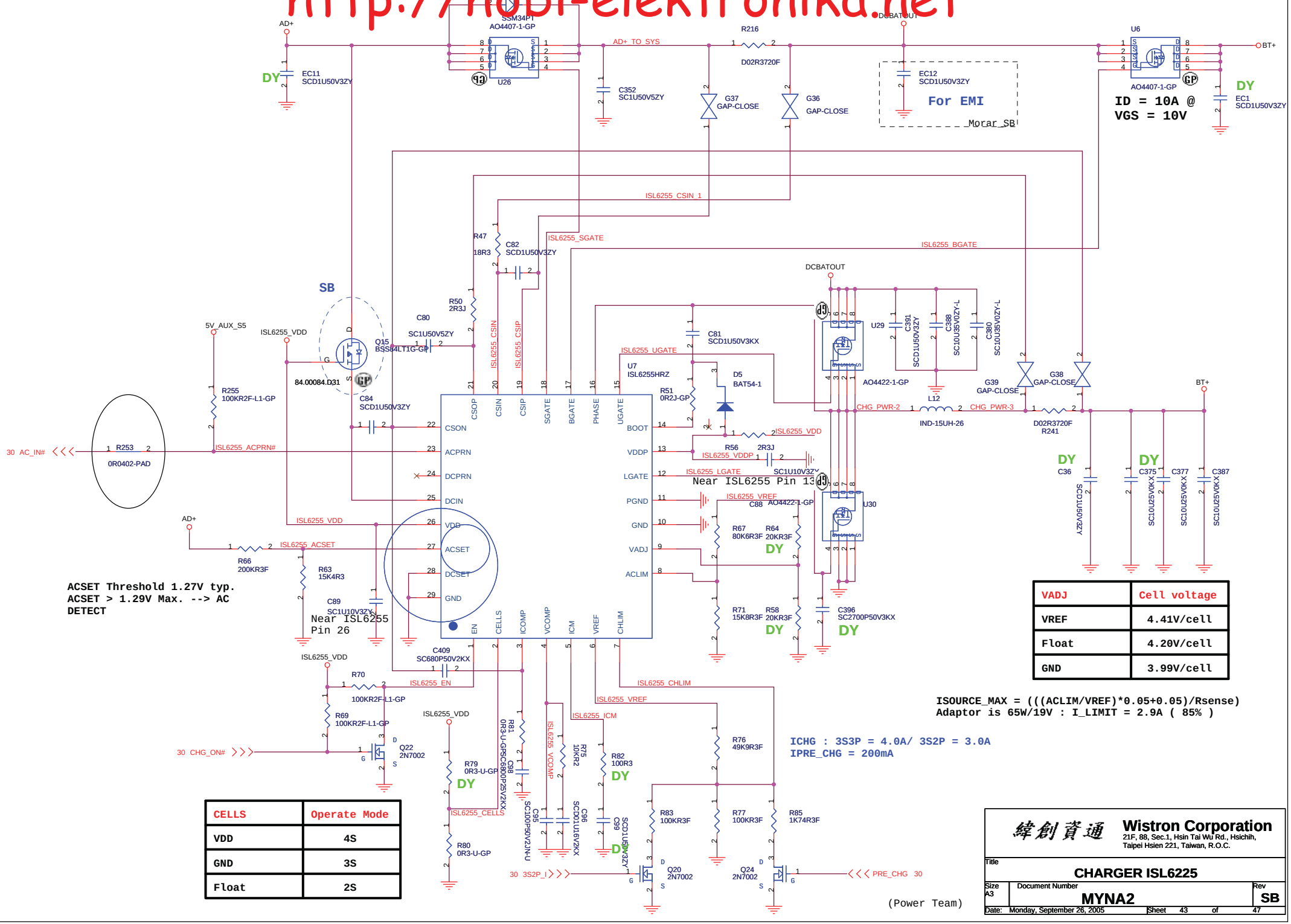

VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

Wistron Corporation	緯創資通
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Title: CHARGER ISL6225	
Size: A3	Document Number: MYNA2
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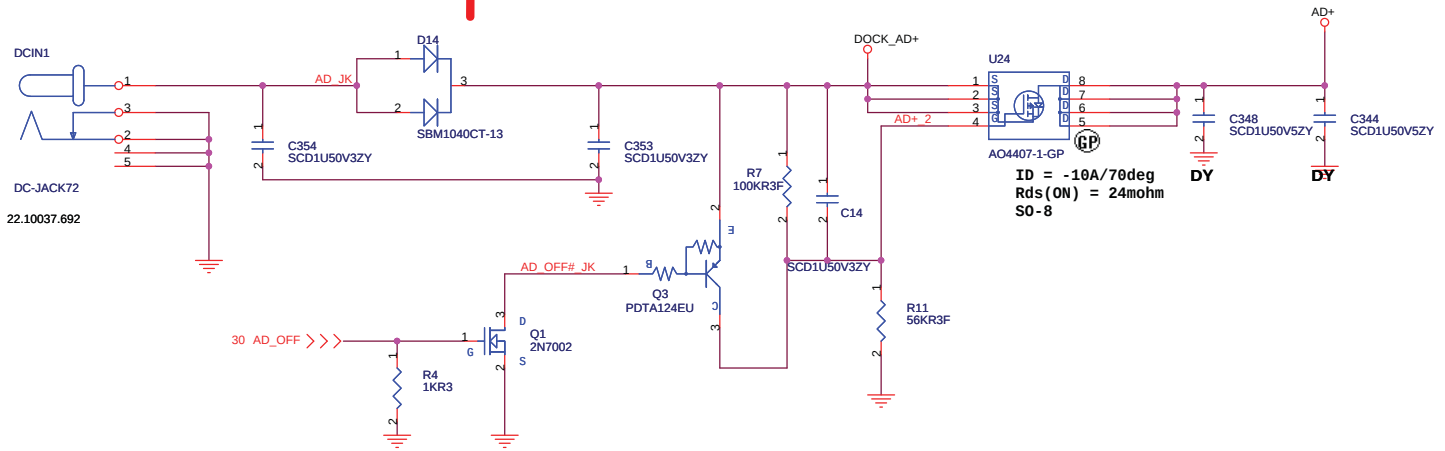
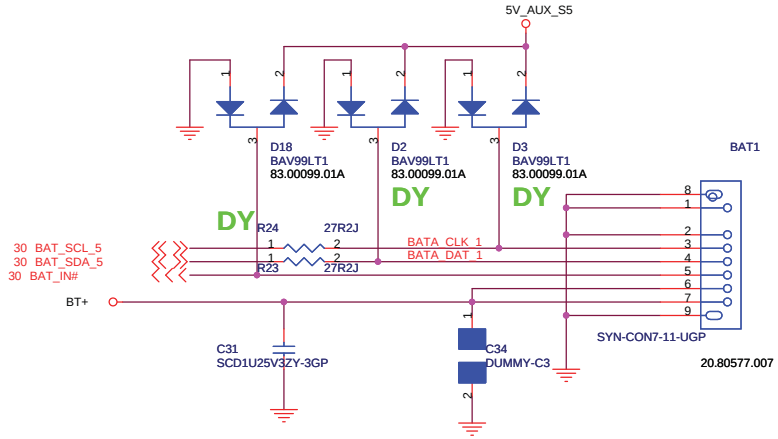
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***AD/BAT CONN***	
Size A3	Document Number Myna2	Rev SB
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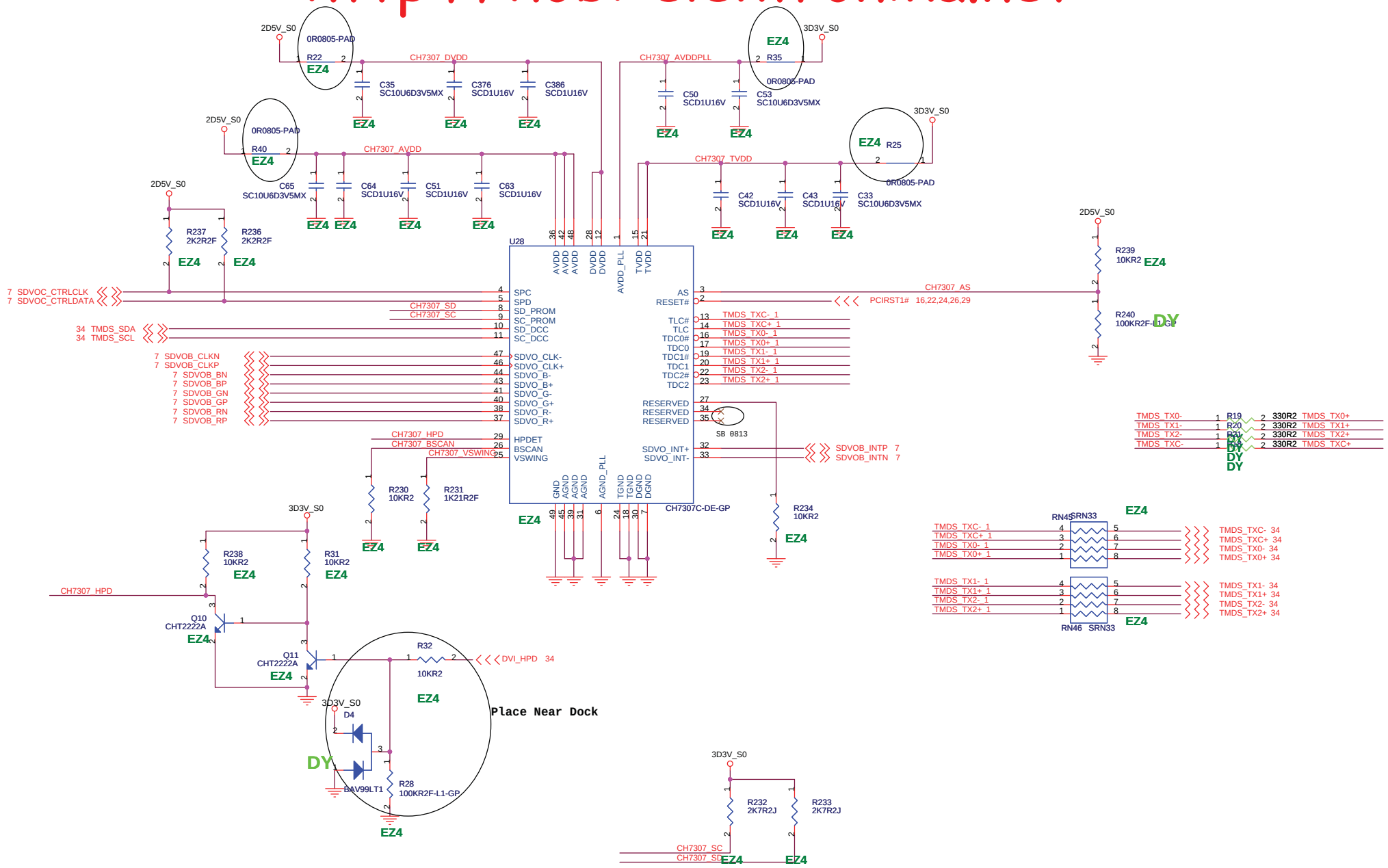

<variant_name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DVI Transmitter-CH7307C

Size: A3 | Document Number: Myna2 | Rev: SB

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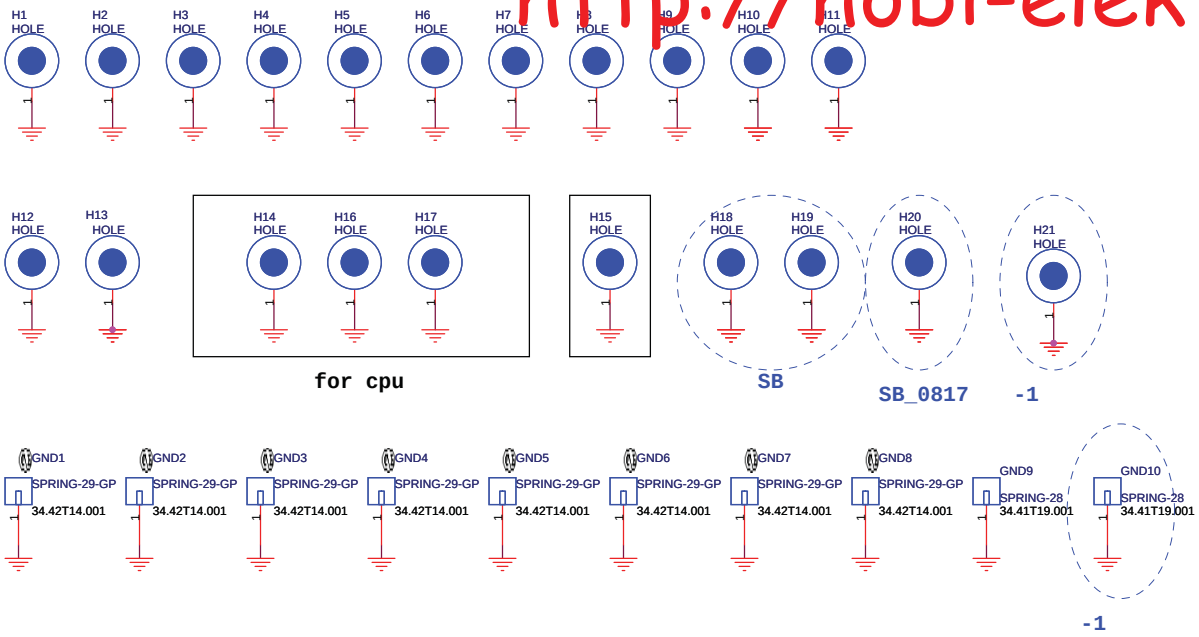

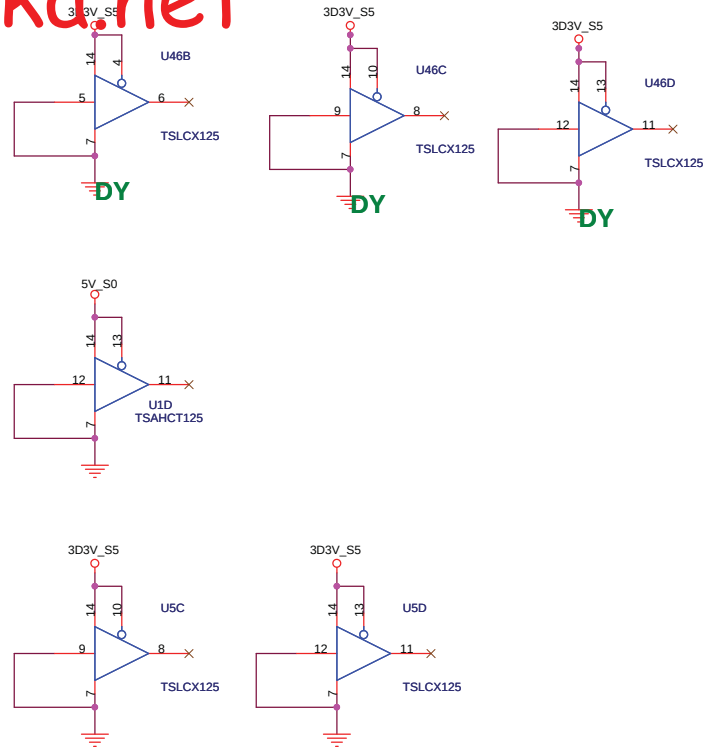

<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SPRING,BOSS & UNUSED TTL***

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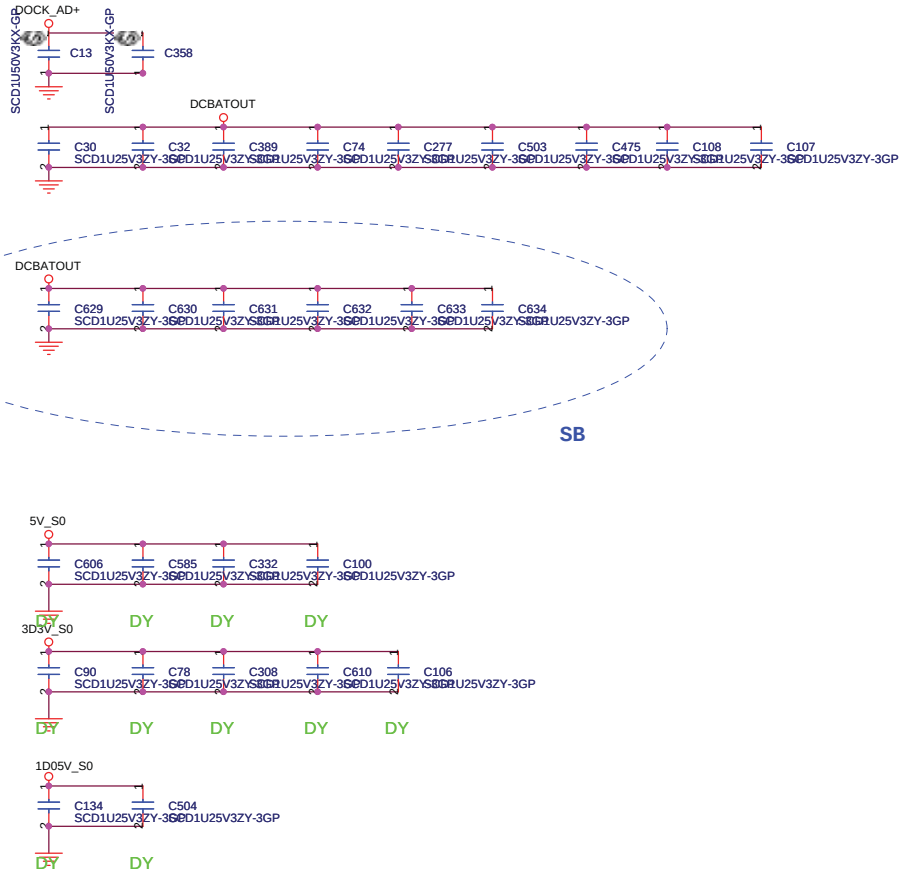

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***EMI SOLUTION***
Size: A3	Document Number: Myna2 — Rev: SB
Date:	Sheet Monday, September 26, 2005